Enhanced photomask quality control by 2D structures monitoring using auto image-to-layout method on advanced 28nm technology node or beyond

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Abstract

As device features continue to shrink, achieving acceptable yields becomes increasingly challenging. In the photolithography process, mask error is one of the most critical error sources, since any imperfections on a mask will be amplified and transferred onto a wafer due to Mask Error Enhancement Factor (MEEF) [1]. Furthermore， due to complexity of lithography optical proximity effect correction in advanced technology nodes, more and more 2D structures are applied into mask patterns. Furthermore, more 2D pattern configurations are susceptible to pattering failures due to their much high MEEF factor than 1D pattern. As a result, the conventional mask error control mechanisms for 1D [2] [3] [4] only, such as mean-to-target (MTT) and CD uniformity, are no longer adequate to deal with high MEEF 2D structures.

In this paper, a novel 2D structure mask error monitoring technique is introduced to prevent fatal wafer printing errors such as CD error, line-end pull back and other pattern distortions to ensure high quality mask manufacturing and to improve wafer yield in advanced technology nodes. We will demonstrate the flow using typical 2D structure test patterns in 28nm technology node design or beyond. The SEM image would be taken and measured by this novel technique are used to monitor mask fidelity performance.

This monitoring technique is based on Image-to-layout, as one of Anchor Semiconductor's pattern centric techniques, which can extract contour and convert it into pattern layouts from SEM or optical image of masks. Further pattern signature analysis can be performed on the pattern (inner /outer vertex, space distance and edge distance), so that we can quickly identify target locations for 2D pattern measurements. We monitor the severity of 2D corner rounding on selected 28nm design rule masks by Pattern Fidelity (PF) ratio and correlate them with wafer printing results.

2D pattern measurement techniques and PF ratio monitoring system from SEM image is an effective approach to ensure high quality mask making in 28nm and advanced technology nodes. This PF ratio monitoring from 2D pattern SEM images is an effective approach to ensure high quality mask making in advanced 28nm node and beyond, which can overcome the inadequacy of current 1D measurement only method, especially for the masks are generated without source mask optimization (SMO) [6].

Key words: 2D structure, image-to-layout, 28nm node, PF ratio, pattern fidelity, MEEF, mask quality

Introduction

As the most critical and (by far) the most complicated operation in all of IC processing, lithographic process has been a key enabler for the technology advances in IC manufacturing for several decades and will continue to be so for the foreseeable future. Mask fabrication process, as one of the most critical components in image transfer from design to wafer through lithography process, is facing ever challenging requirements from lithography. With the dramatically shrinking pattern size and tightened error budget, any imperfection on a mask will be amplified due to Mask Error Enhancement Factor (MEEF) and transferred to fatal error on a wafer.

For 28nm and beyond technology nodes, masks need not only to achieve higher pattern resolution and critical dimension accuracy, but also to decrease the deterioration of the pattern fidelity in 2D structures at certain sites. Currently, however, there is no quantitative metric to measure 2D pattern fidelity, such as, corner rounding.

In this paper, we will introduce a novel 2D structure mask error monitoring technique where pattern fidelity measurement data are collected and, in an "apple to apple" fashion, compared with internal standard base. The basic flow of this monitoring technique is shown in figure 1.

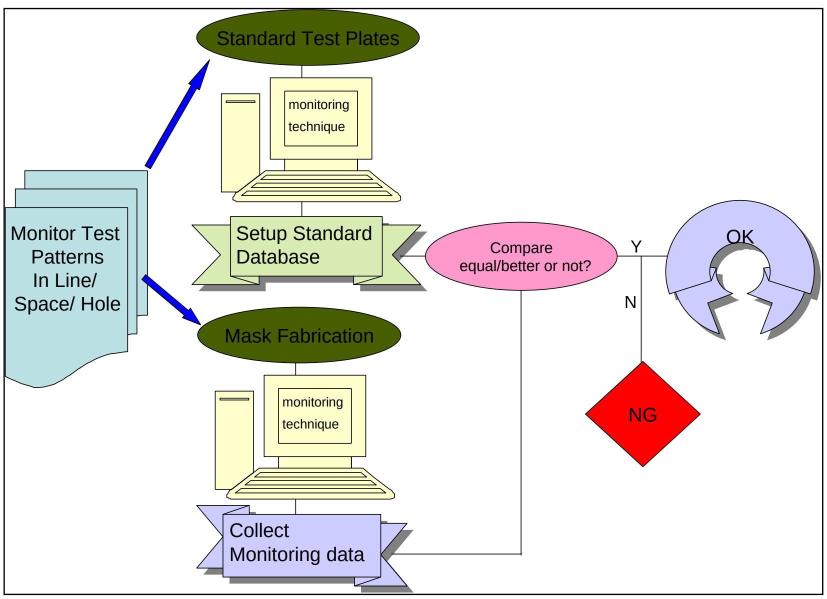


Figure 1: Basic flow used in mask shop

Application Flow

On advanced 28nm technology node and beyond, a mask is judged not only by its pattern resolution and critical dimension accuracy, but also its pattern fidelity at certain reference points. The monitoring of mask fabrication is supposed to be accomplished with the basic flow chart of figure 1. However, pattern fidelity measurement is complicated by the vast number of optical-correction jogs in advanced masks, as the measurement results of conventional metrics would be dramatically affected by difference in pattern size and surrounding environment. It's too hard to provide measurable result with regular ruler and define accurate specification. Therefore, there is an urgent need to have an application flow to monitor pattern fidelity with an acceptable complexity.

We have real data to demonstrate the necessity of pattern fidelity monitoring. Figure 2 shows an example of how wafer CD error is impacted by the difference in mask pattern fidelity. We observe from mask images that small jogs in NG (No Good) Mask #2 are noticeably smaller than good Mask #1. At the same time, Mask #2 also has more serious corner rounding issues. Its wafer CD is about 8% below target in some critical areas, which is not acceptable at 28nm node technology. Since this cannot be detected from normal mask CD result, and these kinds of mask 2D pattern differences are not apparently observed by human eyes from images, nor be accurately measured by CDSEM, we need a new approach to monitor mask quality. With observed correlation between mask pattern fidelity and wafer CD, we choose to use a metrics based on corner rounding, collect measurement data of this metrics at selected pattern corners to monitor the mask pattern fidelity for 28nm and beyond technology nodes.

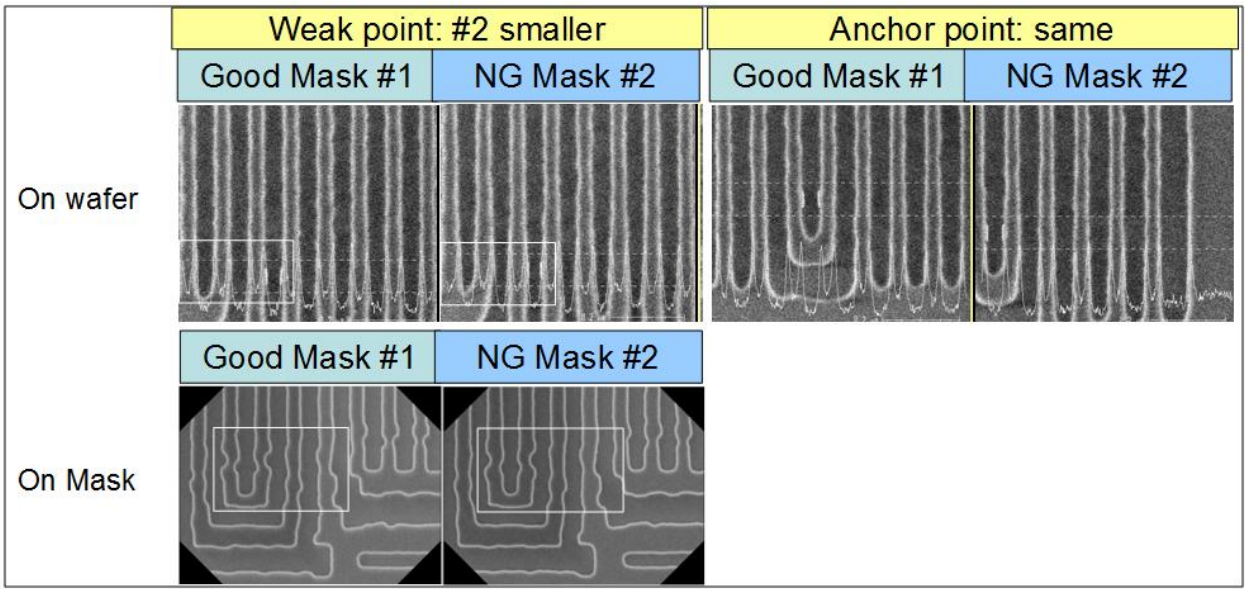


Figure 2: Test Result of wafer CD error due to pattern fidelity issue

In this paper, we introduce this monitoring technique for pattern fidelity in 28nm node and beyond. First, in order to reduce the error's dependency from different test patterns, we define separate monitoring test patterns for different pattern layer and mask process, e.g., separated into dark line negative resist mask, clear line and hole positive resist mask. Secondly, we use multiple test pattern sites to get average and range values, so as to reduce the impact of unknown random factors or to find out possible variations in pattern fidelity on one mask.

Then, we take SEM images of the monitoring test patterns on the acceptable standard masks, then using Image-to-layout to get pattern fidelity results of all selected pattern points. A standard database of pattern fidelity is set up based on these data. During advanced 28nm node mask fabrication, the same monitoring test patterns are put on the masks where pattern fidelity data are collected by the same monitoring technique. As a result, we can compare these data with exist standard database, and determine whether the pattern fidelity on a fabricated mask is acceptable. At the same time, monitor data could also feed back to original database system to calibrate standard database of pattern fidelity for 28nm node mask Technology.

Software Solution

This technique is mainly based on a software Image-to-layout, one of Anchor Semiconductor's pattern centric techniques, which can extract contour and convert it into pattern layout from SEM or optical images of mask. Further pattern signature analysis can be performed on the pattern (inner /outer vertex, space distance and edge distance), so that we can quickly identify target locations for 2D pattern measurements.

Image-to-layout technique is the major technology of this software solution, which can easily detect image signal and convert it to contour or layout as GDS or OASIS format for any other applications [5]. In contour edges, we have different algorithms to detect and allow user to place edges at different position based on design layers such as inner edge, outer edge or 50% threshold position. Once user would like to convert contours to layout patterns, the converted patterns can be all straight lines or include 45-degree lines as well. The figure3 shows a simple case of edge extraction and layout extraction results.

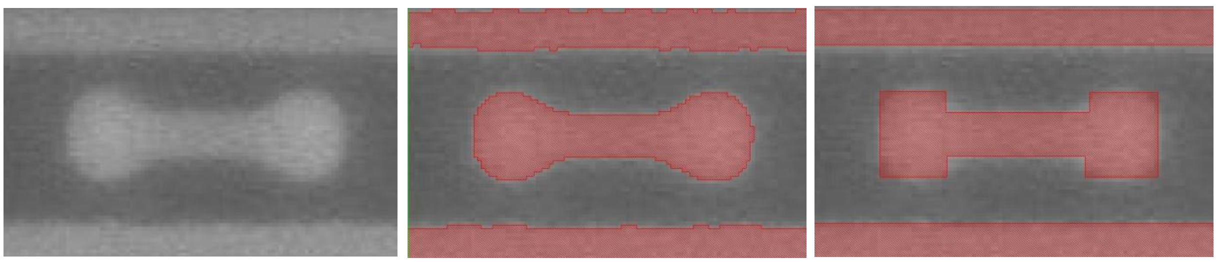
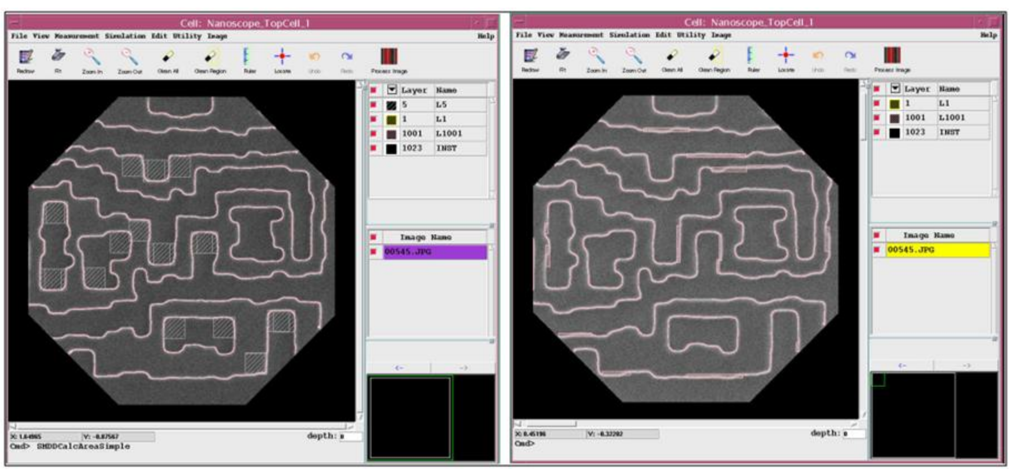


Figure 3: Image to layout techniques can convert image to contour or layout in GDS or OASIS format

We monitor the severity of 2D corner rounding on selected 28nm design rule masks by Pattern Fidelity (PF) ratio and correlate them with wafer printing results. The maximum of corner rounding radius (MR) and its corner extension (E), which is a user-definable parameter, are used to formulate PF ratio. When a polygon's line end width is less than the total distance of MR and E, its corner will not be used for PF measurement. The remaining outer corners will be selected and their PF ratios are calculated as follows:

$$PF\ ratio = \frac{\text{The area of selected corner within the square of (MR + E)}}{\text{(MR + E)^2}} \qquad (1)$$



(a) Extracted contour & selected corners for PF ratio calculation (b) Extracted contour

Figure 4: 2D SEM images GUI- image contour and edge extraction.

If the contour of a corner is perfectly matched with the polygon corner in a layout, then its PF ratio is 1 (the Maximum of PF ratio). The closer of PF ratio to 1, the higher pattern fidelity and mask quality will be.

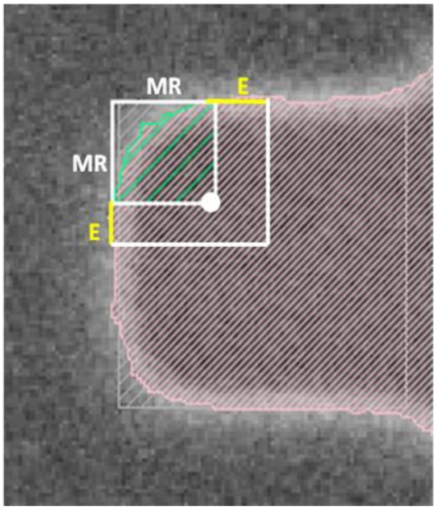


Figure 5: PF ratio measurement

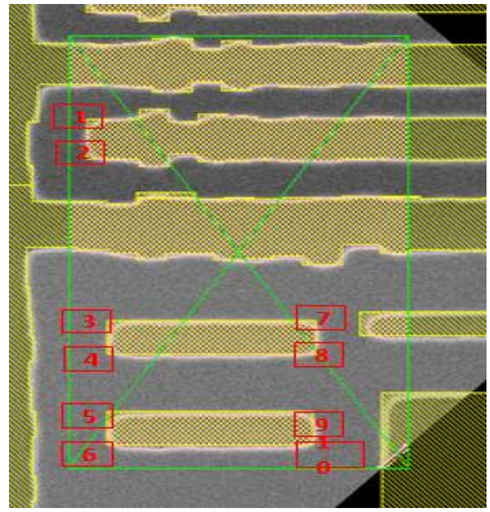


Figure 6: Selected 2D patterns by Image-to-layout

Returning to the two masks mentioned in figure 2, in addition to conventional 1D monitoring of CD mean-to- target, CD uniformity and CD range control, 2D corner rounding severity is also measured at the same corner locations for two masks which are from different E-beam writers. At a total of 10 corners, For Good Mask #1, average PF ratio is 0.783 for Good Mask #1 and 0.728 for NG Mask #2. In terms of their wafer CD mean-to-target, NG Mask #2 is 8% below target while Good Mask #1 is right on target.

During SEM image capture, in order to reduce SEM X-Y distortion, we rotate image capture 45-degree to minimize the image distortion. The 2D measurement images in this paper are all 45-degree captured.

Test Patterns

Test patterns are added into masks for 28nm node and beyond to monitor pattern fidelity. Dark line, clear space and hole pattern masks would have their own test patterns. In this paper, we choose clear space mask as an example to explain the design of test patterns details.

The test patterns are separated into two parts. One part consists of programmed size patterns, which could be detected for the software testing and evaluation. Since corner rounding is used to monitor pattern fidelity, we mainly use hole patterns with different sizes and different pitches. There are 17 hole sizes, ranging from 0.06 to 1um, and 8 pitches, 1:0.8, 1:1, 1:2, 1:3, 1:4, 1:5, 1:10 and fully isolate pattern. After the mask is made, a SEM image with FOV (Field of View) of 3umX3um is taken for each programmed size. These 136 SEM images are then fed into Image-to-layout to get selected corner points and their PF ratio values. These data become a rough database for pattern corner rounding behavior of different size and different environment on the same mask. For the sake of efficiency, not all the patterns are used by the monitoring standard during actual mask fabrication.

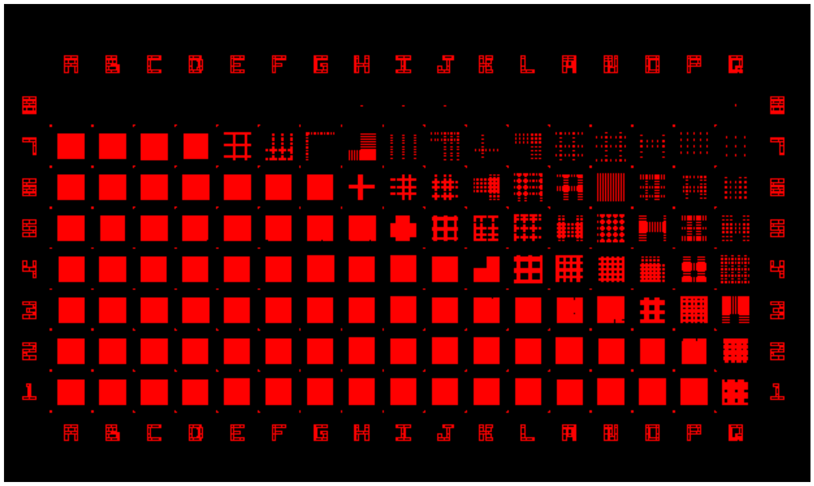


Figure 7: Programmed size hole or island patterns.

The other part consists of some patterns, which are reported by simulation to be possible weak points on wafer. E.g., the test case in figure 2. With the existing wafer test data, we could easily find out how much corner rounding issue on the mask will impact CD on wafer. Moreover, there are some other kinds of patterns, and may be more and more in the future. Our main purpose here is to simulate as many pattern behavior possible which should be very helpful for us to observe and analysis more information on mask fabrication process.

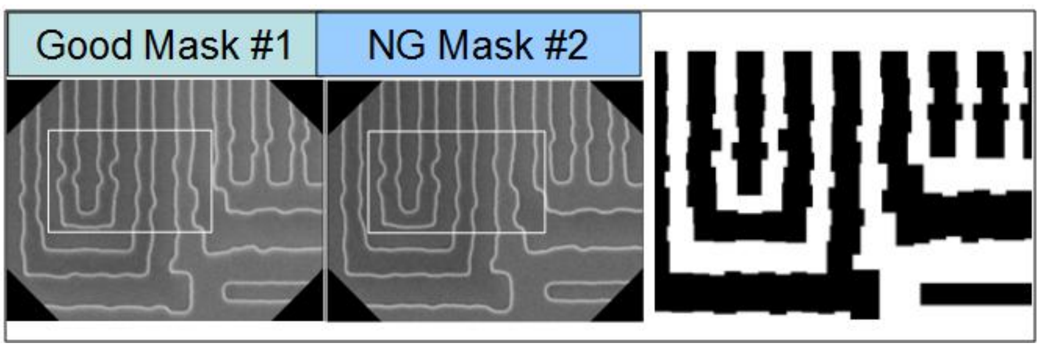


Figure 8: The failure area of figure2 case vs generated test pattern.

These two parts of test patterns would be put into 28nm node mask as default data since they are prerequisites of our 2D structure mask error monitoring technique. Since this technique is still under developing, more reasonable and adaptive version update of the test pattern design is definitely expected.

SEM Image Edge Extraction

As seen from Formula (1), the maximum corner rounding radius (MR) and corner extension (E) are needed to compute Pattern Fidelity (PF) ratio. Figure 4 shows the contour image of Image-to-layout during SEM edge extraction. Figure 8 shows the comparison between polygon fill and the ideal mask patterns (the design GDSII) which can be used to determine the appropriate values for MR and E. The edge extraction algorithm extracts both inner and outer edges from the white edge band due to enhanced edge emission of secondary electrons in SEM images. Depending on the tone selection, either inner edge or outer edge is used. A constant bias can be applied if a user chooses to do so; but in most cases, no bias is needed. After MR and E are determined from comparison with the corresponding GDSII pattern, subsequent PF ratio calculation do not need to involve polygon fill and the GDSII pattern for “apple to apple” comparison of mask pattern fidelity.

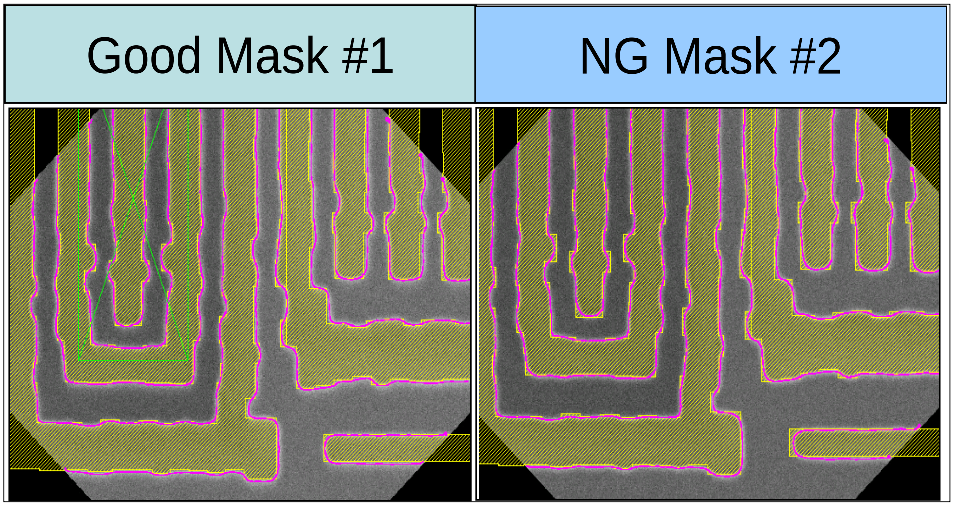
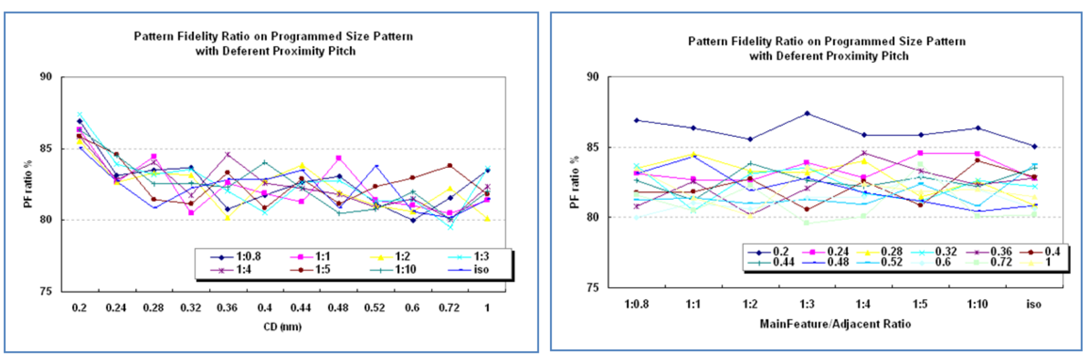


Figure 9: 2D SEM images contour and GDSII reference

Analysis and disposition

Mask pattern fidelity, defined as the corner rounding ratio, is a very sensitive mask error factor. As a result, similar to CD measurements, we need to collect data not only on average, but also on range or 3Sigma in order to be able to correctly judge the mask quality. Therefore, we would like to monitor each corner in all of these test patterns to do data analysis and disposition.

When pattern fidelity Ratio data are collected on a standard mask, test patterns with size of 0.06/0.08/0.1/0.12/0.16um are found to be not usable for reliable pattern fidelity information. Figure 10 shows the data with pattern size ranging from 0.2 to 1um. It is apparent that pattern fidelity ratio is relatively insensitive to proximity pitch. Except for size 0.2um patterns, PF ratio is also relatively insensitive to pattern size. Therefore, these patterns are deemed acceptable as the representative patterns for mask pattern fidelity monitoring.

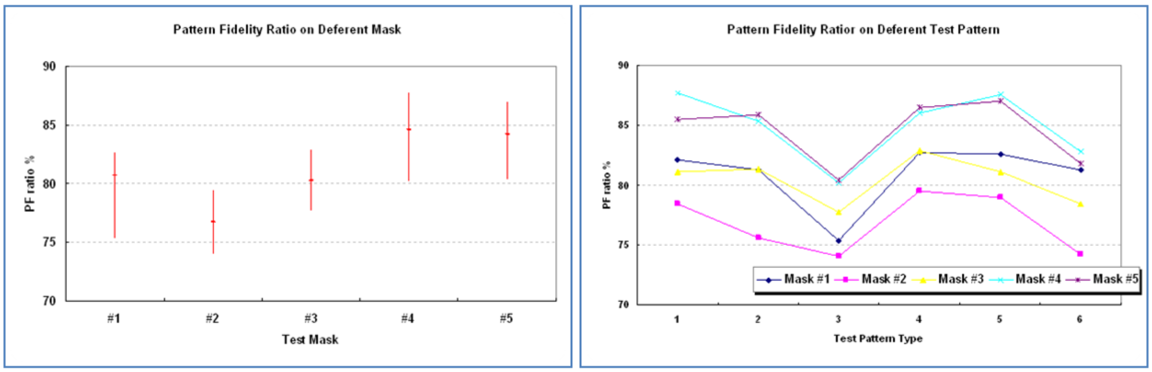


(a) PF behaviors on deferent pitches (b) PF behaviors on deferent size

Figure 10: Data analysis and disposition on programmed size pattern with deferent proximity pitch

Figure 11 shows the result of pattern fidelity ratio measurements for a mask process DOE involving 5 different masks. Mask #1 and mask #2 are the same test masks we mentioned in figure 2 and figure 8, and Mask #1 has been chosen as the standard plate for clear space mask on 28nm node technology. There are six types of test patterns on each mask and 10~20 measurements are performed on each monitoring corners. Although figure 11 (b) shows that PF ratio varies with the test patterns, it also shows that PF ratio of each test pattern type has largely similar trend over different mask. This provides strong support for our 2D structure monitoring technique to be used to in monitoring mask quality.

Based on the comparison with the standard data base of Mask #1, Mask #2 is definitely not a good plate and needs to improve, Mask #3 is equal or maybe a little worse than standard, and both Mask #4/#5 are better than standard.



(a) PF behaviors on 5pcs masks

(b) PF behaviors on 6 types of test pattern (average of all corners)

Figure 11: Data analysis and disposition on 5pcs test masks with 6 types of test pattern

Summary and Future work

We have demonstrated a working software solution for monitoring 2D structure mask error using SEM image of representative designed test patterns and have shown the software solution and application flow. With test patterns of programmed sizes and a collection of weak point similar test patterns, the software can accurately extract the edge of each corner on a test pattern and compute PF Ratios with MR and E selected in reference to the original GDSII. The approximate results of mask pattern fidelity Ratio performance on each mask would be compared to standard database and get the conclusion of pass or not.

This software has been applied in mask fabrication application flow. It offers our mask shop a unique capability for 28nm node and below mask pattern fidelity error analysis and disposition in R&D, as well as in production. This enhanced 2D structure monitoring approach can cover the inadequacy of current 1D measurement in current OPC model, DRC and MRC, especially the masks without source mask optimization (SMO) [6].

The software is currently still under development. We’re searching for most adaptive test pattern to cover as many pattern fidelity behaviors as possible and set up most comprehensive standard database. In addition, this software is semi-automated for application, although the automation requirement is not essential, automation improvement is also planned in the future. It is believed that this software may be extended beyond what has been described here.

REFERENCES

1. Poock et al. “Wafer fab mask qualification techniques and limitations”, Proc. SPIE, Vol. 6349, 63490U (2006)

2. Zait et al. CD Variations Correction by Local Transmission Control of Photomasks Done with a Novel Laser based Process. ML 6152-76 SPIE Microlithography 2006

3. Zait et al. Irradiation Resistance of Intravolume Shading Elements embedded in Photomasks used for CD Uniformity Control by Local Intra-field Transmission Attenuation. PMJ 2006 6283-11

4. Morikawa et al. In-field CD uniformity control by altering transmission distribution of the photomask, using Ultra fast pulsed laser technology. PMJ 2006 6283-29

5. Eric G. Guo, et al, "Simulation based mask defect repair verification and disposition", Proc. SPIE 7488, (2009).

6. Rosenbluth, A.E et al. "Intensive Optimization of Masks and Sources for 22nm Lithography", Optical MicroLithography XXII, Proc. SPIE Vol. 7274 (2009).