DFM: A Practical Layout Optimization Procedure for the Improved Process Window for an Existing 90-nm Product.

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Abstract

As the advent of advanced process technology such as 90-nm and below, the design rules become more and more complicated than before. These complicated design rules can guarantee process margin for the most layout environments. However, some layouts have narrow process windows that were still within the design rules. For example, line end layouts in a dense environment would generally have narrower process window than that of the one-dimensional (1-D) dense line environment. The dense line end spacing design rule would be larger than that of the 1-D dense line spacing to compensate for the narrow window effect.

In this work, an optical simulation software was used to examine an existing 90-nm FPGA product pre-OPC layout for its optical contrast. The optical contrast could correlate to the depth of focus (DOF) process window. Several back end locations were identified with possible narrow DOF windows. From the evaluations of these low contrast patterns, several design for manufacturing (DFM) rules and DRC deck was then developed. This deck effectively identified the narrow process window layout locations, previously found with the simulation software. These locations were then optimized for the improved DOF windows.

Both simulation and in-line data showed that the DOF window was improved after the layout optimization. Product data with optimized layouts also showed the improved yield.

Key words: DFM, OPC, MEEF, Lithography.

Introduction

For the technology node of 130 nm or earlier, product layouts followed design rules could generally have large process windows and good tolerance of process variations. For 90-nm technology node and below, due to the increased optical proximity effect, caused by the tightened pitches and complex two-dimensional (2-D) patters, design rules could only ensure reasonable process windows and tolerance of process variations. The process window could be affected by bad layout styles such as un-necessary jogs or complex 2-D patterns with minimum space and wide CD. Therefore, implementation of a layout inspection and optimization procedure at the pre-tapeout stage would be needed to reduce bad layout pattern counts.

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In this work, such a procedure was implemented for optimizing a pre-OPC layout of a 90-nm product for the improved lithographic process DOF window, without increasing the chip size. Layout modifications through this procedure could also provide OPC friendly layout environments.

In this procedure, an optical simulation software was used to calculate the optical contrast of the product layout and generated a contrast versus occurrence distribution for each layer. The low contrast layout environments, which highly impacted the DOF window, were then identified from the contrast distribution of the layer. With aids of the simulation software, the optimized layout modifications that had best DOF improvement were obtained and implemented.

To categorize the low contrast patterns, several design rules were derived based on the layout contrast analysis. These rules also helped to locate the layout patterns that could be modified for the DOF window improvement in other product layouts of the same technology generation.

For the modified layouts, the simulation data clearly showed the increased contrast and the improved DOF window. The experimental data also drew a similar conclusion to that from the simulation.

The approach

Under a fixed illumination wavelength, the diffraction effect (i.e., light diffraction angle passing through the layout patterns in a mask) of 2-D patterns such as line ends and corner patterns is stronger than that of 1-D patterns[1]. The strong diffraction effect causes low optical contrast and poor image quality. The low optical contrast could also result in a narrow DOF process window[2].

An existing 90-nm product full-chip pre-OPC layout was examined by the optical simulation software with focuses on dense and semi-dense layout patterns. The iso-patterns could be fixed by OPC to achieve optimized process windows and were precluded in this analysis. The simulated optical contrast distribution for such pattern densities described above shown in Figure 1.

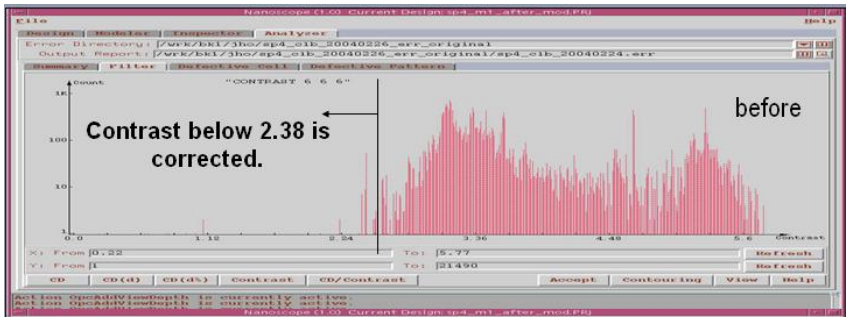

Figure 1: Optical contrast distribution before layout fix.

Low optical contrast patterns were then analyzed for systematic pattern similarity that caused the low optical contrast. This simple approach could help to systematic identify patterns that had narrow process window. Several design for manufacturing (DFM) rules were then derived from this analysis. The rule deck then flagged the low contrast locations for subsequent analysis and fixes.

The design for manufacturing (DFM) rules

The full-chip simulation of the product layout revealed that fixable low contrast patterns could be attributed to the following categories:

1. Dense line patterns with available space nearby to enlarge the line-to-line space.
2. Dense line end patterns with available space nearby to enlarge the line-to-tip space.
3. Dense wide line pattern in which the wide line width could be reduced to enlarge the line-to-line space.
4. Dense wide line-to-tip pattern in which the wide line width could be reduced to enlarge the line-to-tip space.

The Figures 2A, 2B, 2C, and 2D illustrated the layout patterns that could potentially have low process windows and could be improved by minor layout optimization.

As could be seen in Figures 2A and 2B, the line pattern with minimum space S1 and wide space S2, the line could be shifted to a wide space S2 direction so that the dense space S1 could be relaxed. This minor modification could improve the DOF of the dense pattern. For line-end dense pattern, this could yield a large space for OPC correction.

For narrow-wide or wide-wide dense patterns, the wide pattern width,W1, could be optimized to yield space for the dense environment. Fox example, as shown in Figure 2C, the wide pattern width W1 could be reduced to yield a larger space, S, for the adjacent pattern. As another example in Figure 2D, the reduced pattern width W1 could enlarge the line end space for an OPC friendly environment.

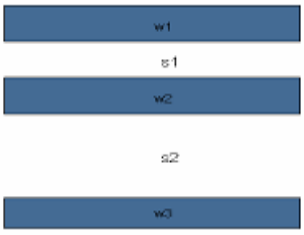

Figure 2A: Type 1 pattern with unequal space line pattern with a minimum space S1.

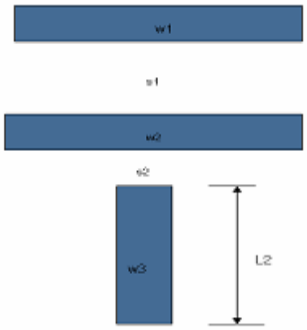

Figure 2B: Type 2 pattern with unequal space line-to-tip pattern with a minimum line-to-tip space S2.

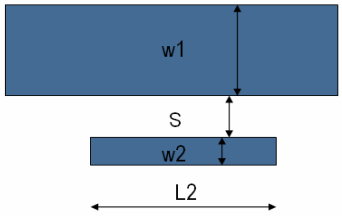

Figure 2C: Type 3 pattern with wide-narrow line pattern with a minimum space S.

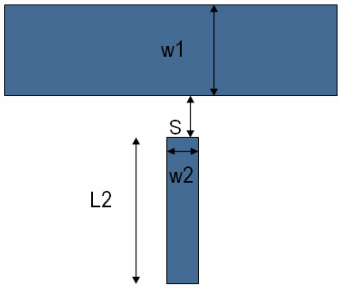

Figure 2D: Type 4 pattern with wide-narrow line-to-tip pattern with a minimum space S.

With a proper DRC deck having the above rules implemented, the metal 1 and metal layers of a Xilinx 90-nm product layout was checked. Typical flagged layout patterns of Type 1 and Type 2 were shown in the Figure 3A. The DRC deck flagged patterns of Type 3 and Type 4 were shown in the Figure 3B and Figure 3C.

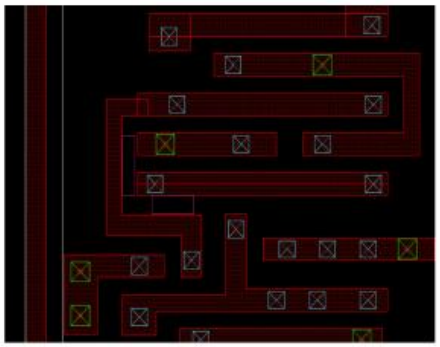

Figure 3A: Type 1 and Type 2 patterns before fix.

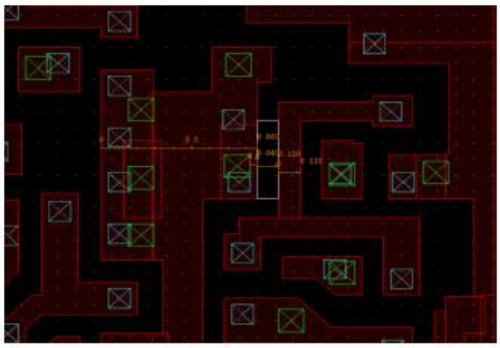

Figure 3B: Type 3 pattern before fix

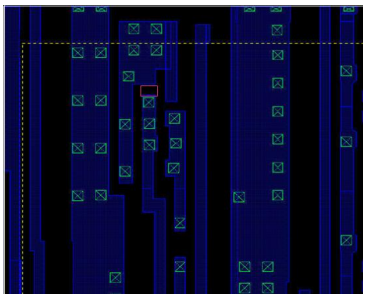

Figure 3C: Type 4 pattern before fix.

After the layout fix results.

In this work, the typical DRC flagged patterns, after optimizations, were shown in the Figures 4A, 4B, and 4C. The layout pattern modifications took environment restriction as well as simulated DOF, and optical contrast into considerations.

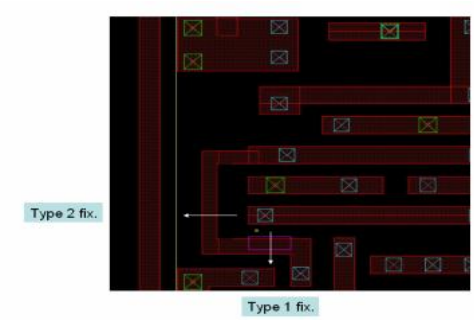

Figure 4A: Type 1 and Type 2 patterns after fixes in which the line spaces were equalized and line end space was enlarged.

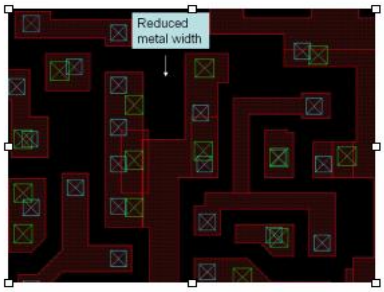

Figure 4B: Type 3 pattern after fix.

Figure 4C: Type 4 pattern after fix.

In this work, most low contrast patterns involved single layer layout modifications for the improved process window. For the SRAM cell in the FPGA, local metal 1 interconnect modification involved additional (diffusion, poly, and contact) layers. Figure 5 illustrated the layout modification steps:

1. Move the diffusion leftward.
2. Move contact leftward.
3. Modify poly-to-contact enclosure.
4. Cut the metal 1 to increate the metal line end spacing (A).

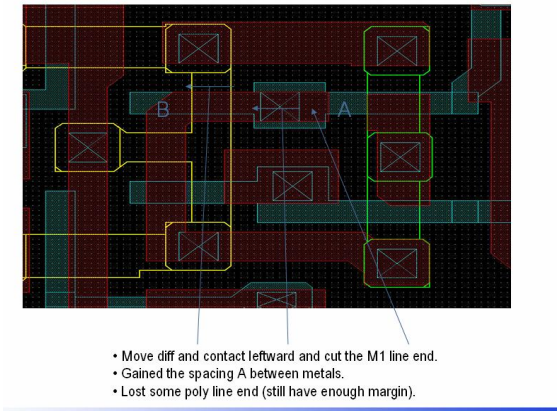

Figure 5: Illustration of a memory cell layout fix procedure.

Simulation results

After these modifications, the full-chip optical contrast was simulated again. Comparing the optical contrast distribution in Figure 1, with Figure 6 as shown below, the minimum optical contrast in the calculated distribution after layout optimization was shifted from 0.5 to greater than 2.38. These low contrast patterns were modified and the process window improvement was apparent. Due to the fact that this work did not change the chip size or relax the ground design rules such as line-to-line space, only certain layout patterns with the low optical contrast were considered for modifications.

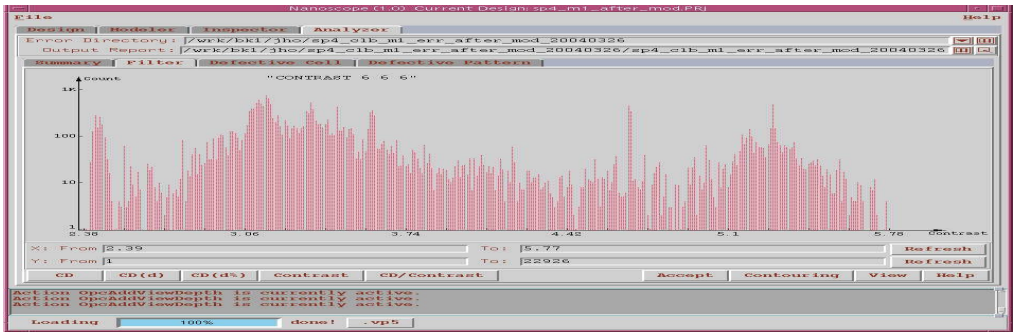

Figure 6: Optical contrast distribution for the layout after fix and the minimum optical contrast was 2.38 and it was 0.5 for the layout before fix.

DOF and image contours of several low contrast patterns were simulated with the software. For the low contrast patterns identified, the narrow space was relaxed by moving the patterns to the locally available space. As shown in Figure 7A through 7H for the common process window and the image contours for the low contrast layouts before and after fixes, the simulation results showed an improved process window. For the dense and semi-dense patterns, modifications of the pre-OPC layout could also lead to post-OPC layout process window improvements.

In these simulations, both S1 and S2 were considered for determining the common process window. For the pattern before fix, the S1 process window was smaller than S2. After fix, as shown in Figures 7C and 7D, the S2 window became smaller than S1's window. However the common window for S1 and S2, after fix, became larger than that of before fix.

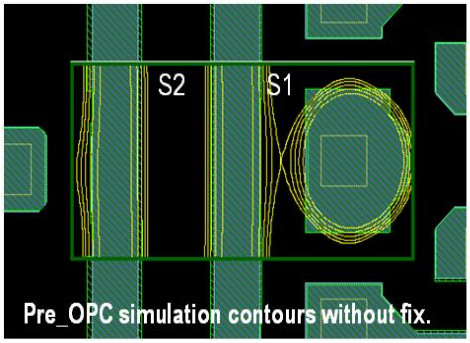

Figure 7A: Simulated image contours of pre-OPC layout before fix.

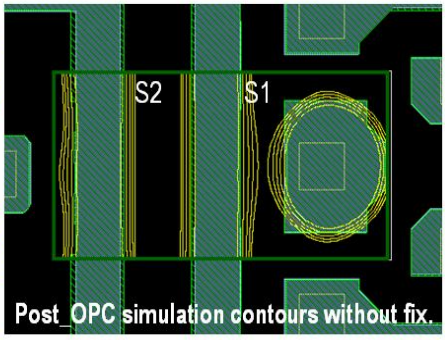

Figure 7B: Simulated image contours of post-OPC layout before fix.

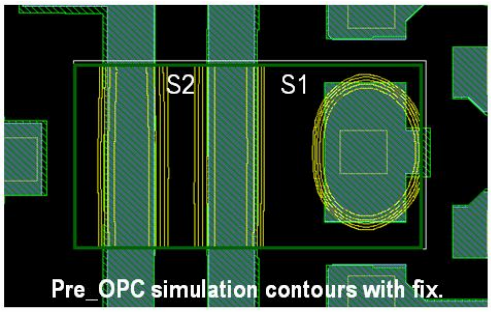

Figure 7C: Simulated image contours of pre-OPC layout after fix.

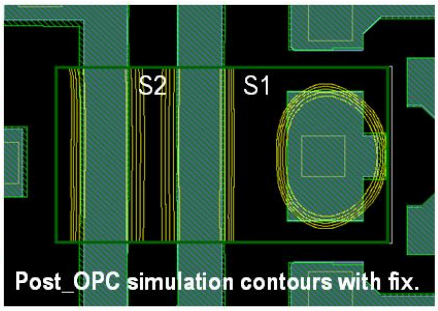

Figure 7D: Simulated image contours of post-OPC layout after fix.

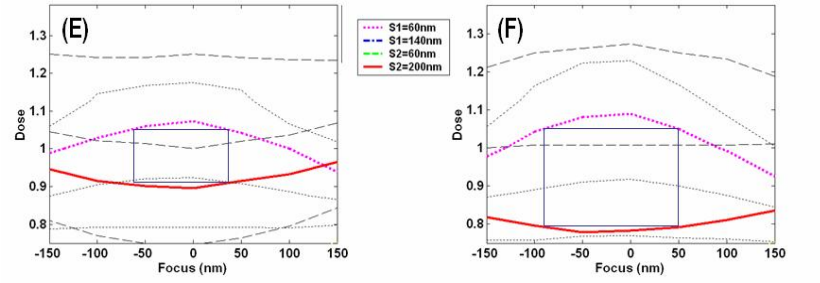

Figure 7E: Simulated process window for the pre-OPC layout, before fix.

Figure 7F: Simulated process window for the post OPC layout before fix.

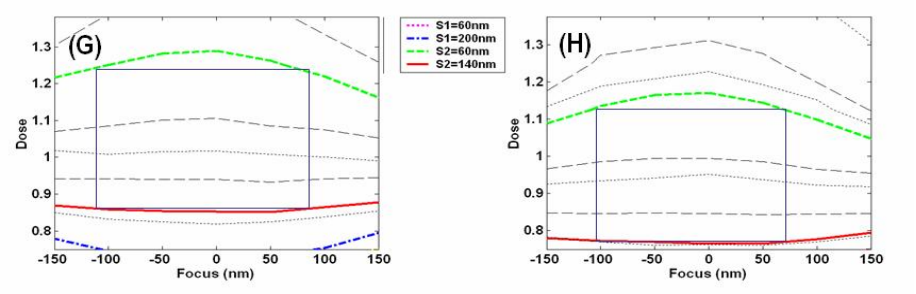

Figure 7G: Simulated process window for the pre-OPC layout after fix.

Figure 7H: Simulated process window for the post-OPC layout after fix.

In-line experimental data

The low contrast locations in the layout were checked in-line with both baseline and 0.1 um defocus conditions. As shown in Figure 8, 9, and 10, it could be seen clearly that the CD variations under the defocus condition was smaller for the fixed layout than that without fix.

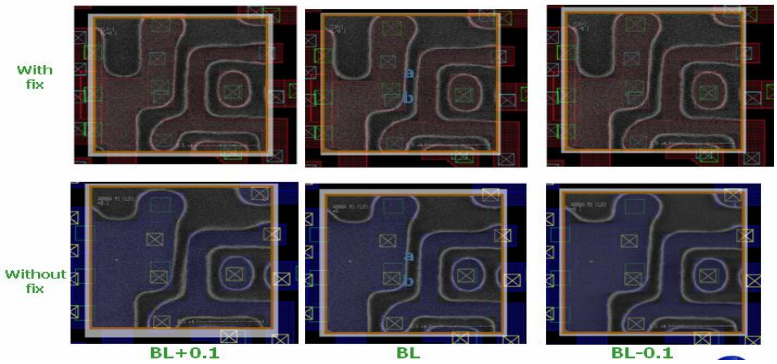

Figure 8: in-line ADI SEM pictures (overlaid with drawn layouts) for Type 3 low contrast patterns before and after layout fixes. It could be clear seen that without fixed pattern showed a smeared photoresist at the location marked b above. The fixed layout pattern did not show this problem under DOF condition.

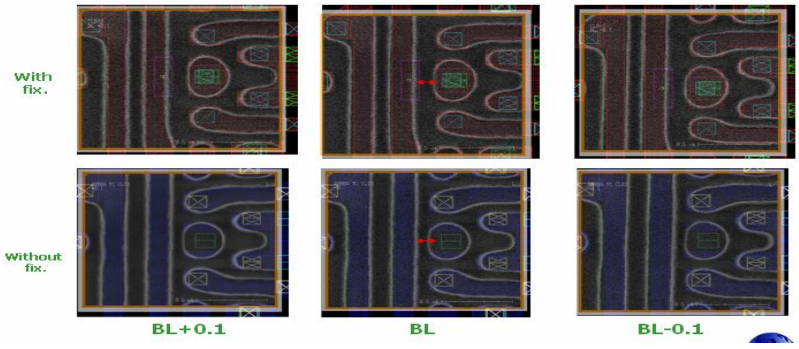

Figure 9: in-line SEM pictures for a Type 2 low contrast pattern. The modified location as marked with an arrow sign showed a large space under the DOF (-0.1 um) condition. The pattern without fixed showed a minor smear image (spread white line) along the line.

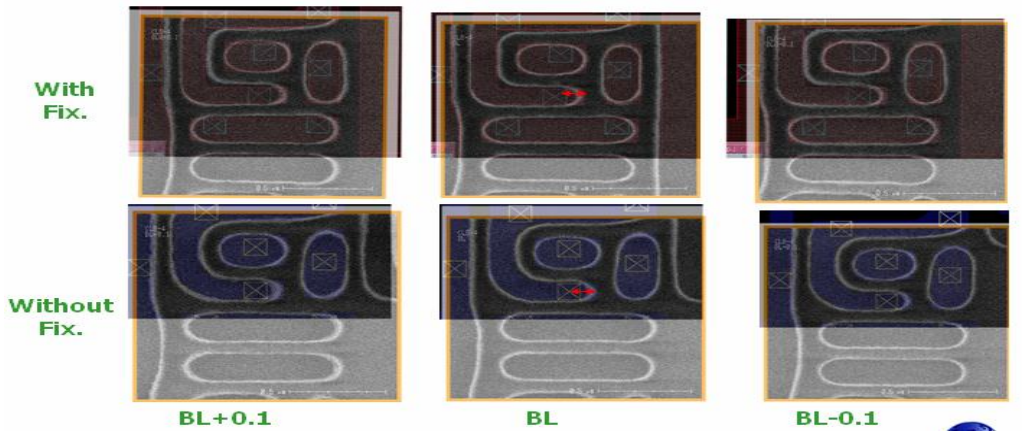

Figure 10: the memory cell line was enlarged for the fixed pattern as indicated by the arrow sign. It could be seen clearly that under the DOF condition the line end was shortened (also resist image smeared) more for without fixed pattern than that with fixed pattern.

The CD's measured from the above in-line SEM data were summarized as the Table 1. It could be clearly seen that, judging from the measured CD variations under baseline (BL) and defocus (BL +/- 0.1um) the modified layout pattern process windows were improved.

Location	Product	BL-0.1um	BL	BL+-0.1um
Figure 8/Location "a"	SPYG	0.08	0.08	0.08
	BYZ	0.075	0.075	0.075
Figure 8/Location "b"	SPYG	0.09	0.09	0.09
	BYZ	0.05+	0.075	0.075
Figure 9	SPYG	0.1	0.1	0.1
	BYZ	0.06	0.075	0.06
Figure 10 (memory cell)	SPYG	0.05+	0.05	0.05
	BYZ	0.025	0.05-	0.05-

Table1: Summary of the in-line SEM CD measurements. The table indicated clearly that, judging from the measured CD's, the modified patterns showed an improved process window.

Product test results

This existing product was taped out after the DFM layout pattern optimizations and DFM memory cell design retargeting. The memory cell failure trend chart for the products with and without DFM fixes was shown as Figure 11. The DFM fixed product showed a stable failure rate, averaged 8.8%, while the without DFM fixed product showed higher failure rate at about 11%. Also, from the Figure 11, the memory cell failure fluctuation was less for the DFM fixed results than the product without DFM fixes (standard deviation: 0.67% with DFM fixed product versus 1.77% without DFM fixed product).

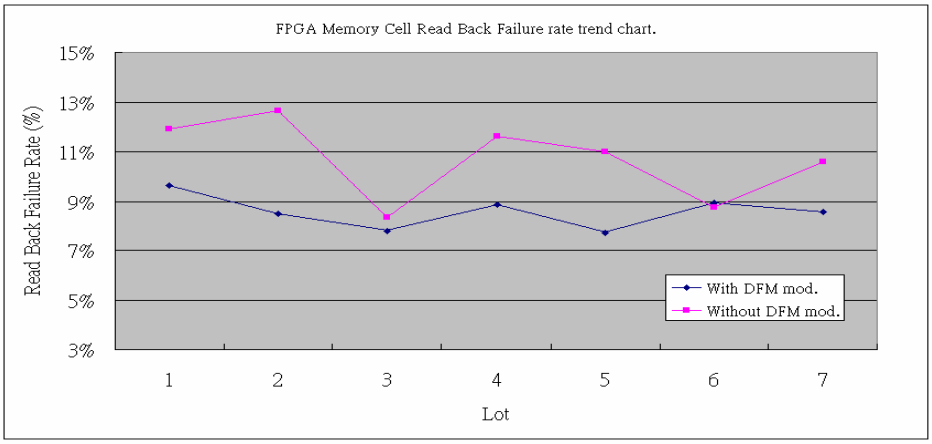

Figure 11: FPGA memory cell failure rate trend chart.

Conclusion

Sub 100 nm process technology such as the 90-nm process technology had more complicated design rules than that from the previous process technology generation such as 130 nm. Product design followed the design rules still could not always have guaranteed process windows.

In the work, an optical simulation tool was used to examine the optical contrast of a 90-nm product layout for potential weak process window patterns. Several design for manufacturing (DFM) rules were derived from the simulation results. A DRC deck with the DFM rules implemented efficiently flagged the full-chip patterns for review and fix.

The simulation of the fixed layout showed an increased optical contrast. In-line SEM CD measurements also showed the reduced CD variations for the fixed layouts under the defocus conditions.

The FPGA memory cell read back failure trend chart revealed a reduced failure rate for the DFM fixed product than that of the product layout without the DFM fix.

References

1. Joseph W. Goodman, “Introduction To Fourier Optics”, Chapter 4, pp 57-73, McGraw-Hill Physical and Quantum Electronics Series, 1968.
2. Chris A. Mack, “Using the normalized image log-slope Part 2”, Microlithography World, pp. 20-22, May, 2001.