# Yield impacting systematic defects search and management

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## ABSTRACT

Despite great effort before design tapeout, there are still some pattern related systematic defects showing up in production, which impact product yield. Through various check points in the production life cycle endeavor is made to detect these defective patterns. It is seen that apart from the known defective patterns, slight variations of polygon sizes and shapes in the known defective patterns also cause yield loss. This complexity is further compounded when interactions among multiple process layers causes the defect. Normally the exact pattern matching techniques cannot detect these variations of the defective patterns. With the currently existing tools in the fab it is a challenge to define the 'sensitive patterns', which are arbitrary variations in the known 'defective patterns'. A design based approach has been successfully experimented on product wafers to detect yield impacting defects that greatly reduces the TAT for hotspot analysis and also provides optimized care area definition to enable high sensitivity wafer inspection.

A novel Rule based pattern search technique developed by Anchor Semiconductor has been used to find sensitive patterns in the full chip design. This technique allows GUI based pattern search rule generation like, edge move or edge-to-edge distance range, so that any variations of a particular sensitive pattern can be captured and flagged. Especially the pattern rules involving multiple process layers, like M1-V1-M2, can be defined easily using this technique. Apart from using this novel pattern search technique, design signatures are also extracted around the defect locations in the wafer and used in defect classification. This enhanced defect classification greatly helps in determining most critical defects among the total defect population. The effectiveness of this technique has been established through design to defect correlation and SEM verification.

In this paper we will report details of the design based experiments that were successfully run on multiple process layers in production device.

Keywords- defects, rule based pattern search, care area, wafer inspection, SEM image, PWQ wafer

## INTRODUCTION

Various studies have been carried out to transfer the design knowledge to manufacturing to enable process engineers monitor and detect pattern related defects [1, 2]. It is found that exhaustive knowledge and tools for design based hotspot determination is limited to the design community. Though the wafer manufacturing checkpoints can find the real defects but in the absence of the appropriate tools and knowledge they cannot utilize the information to find the hidden yield impacting defects efficiently. We report here a successful novel approach to utilize design information and detect new systematic defects on wafers. Known killer defects identified from SEM review or failure analysis have been used as templates to define the hotspot pattern rules utilizing multi-layer design layout; a new proprietary rule based pattern search technique is used to find more hotspot patterns sharing the same or similar pattern properties and the search result is then propagated to wafers for improving defect capture and monitoring.

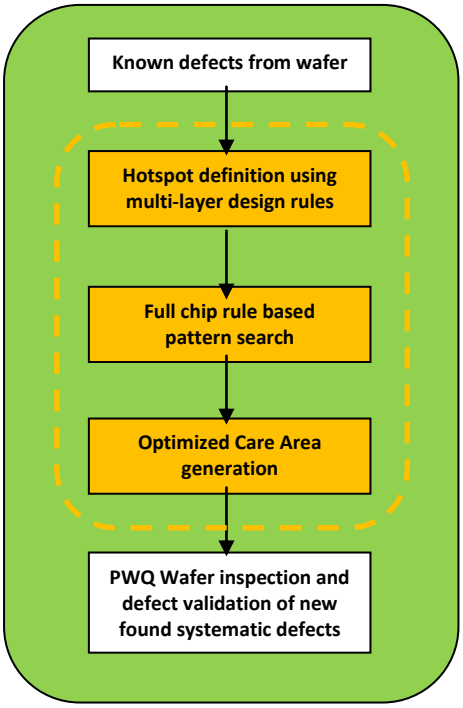



*Figure 1: Application flow chart of new approach*

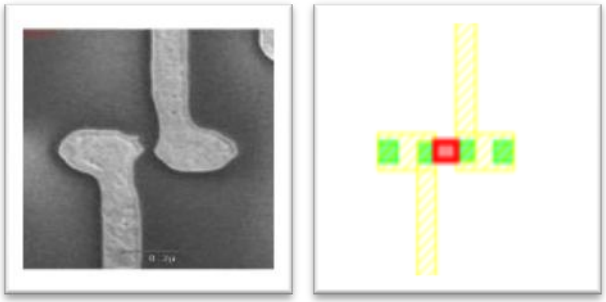
In this paper, we report the results with the new approach on 55nm and 65nm technology nodes devices. The Anchor Semiconductor® proprietary rule based pattern search algorithm has been used during this project. The procedure adopted for each stage of this experiment has been elaborated and substantiated by real manufacturing data.

As shown in Figure 1, we first selected known killer defect from known devices mentioned above; we them locate them in the corresponding design layout and clip out defect patterns. In the following step we define the hotspot pattern rules for those known wafer defects using GUI based pattern rule editor, then conduct full chip pattern search using newly developed rule based pattern search technique. The pattern search result is then used to optimize the care area for the wafer inspection recipe. In this study we use sensitive PWQ wafer to enhance the process variation. Finally we correlate the PWQ wafer inspection result with the pattern search result and validate the correlated defects using SEM review.

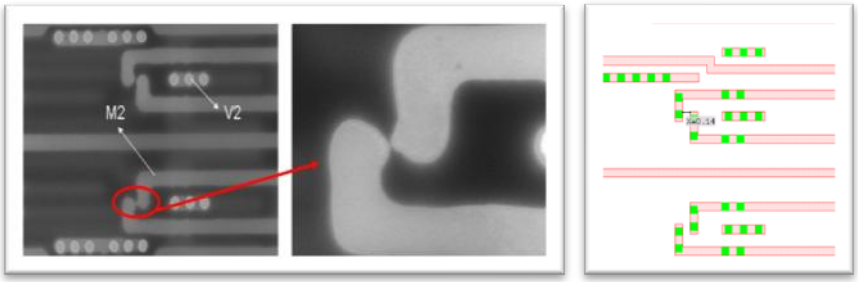
## KNOWN DEFECTS AND HOTSPOT PATTERNS

There are various check points during wafer manufacturing process to detect systematic and random defects and continuously reduce them through process improvements. During the lifecycle of the device development-pilot-production a library of known defects is generally generated and maintained for critical layers and updated regularly. This library is used to monitor the appearance of yield limiting defects during production and eliminate them if possible to boost the yield. Design layout is generally not available in wafer fabs, the defects are generally saved in image formats, like SEM top view and cross section images.

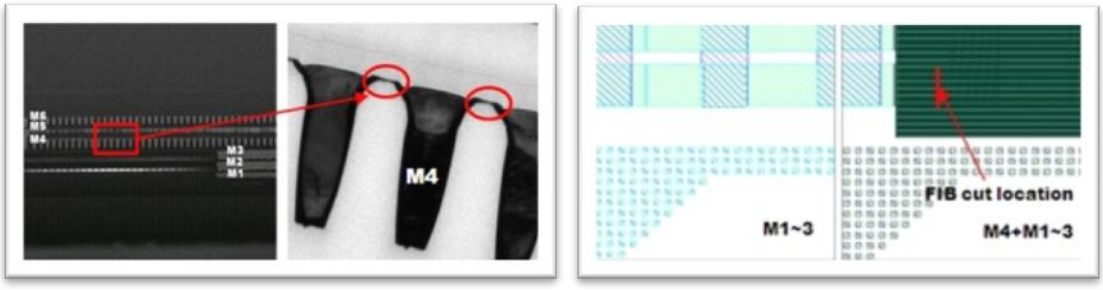
During the process development, the defect library was built for the two devices reported in this paper. Here we use one known defect in the library as an example to generate rules for hotspot pattern definition. The knowledge of exact design parameters is very critical to this step. In normal case, the layout of these known defects should be located and saved in the library together with the SEM images. There are tools available to extract the layout from the SEM images [3]. In absence of the exact design layout for a given defect, user can even draw the pattern clip manually to define the hotspot pattern, as long as the pattern capture the key elements of the defect. The polygon dimensions in the drawn pattern clip are normally determined by design (e.g., design rules) and process knowledge (e.g., critical dimensions).



(a) *Example1 wafer SEM image and layout clip of Via induced metal bridge*




(b) *Example2 wafer SEM images and layout clip of Via induced metal bridge*




(c) *Example wafer cross-section image and layout of Metal bridging*

*Figure 2: Examples of known defects and corresponding layout*

Figure 2 illustrates the examples of known process weak points from wafers and the corresponding layout patterns. In Figure 2(a) and (b) is shown SEM images of the metal bridge that are connected to underneath vias. Corresponding layout revealed that two pairs of closely packed via's under the bridged Metal lines caused the problem. In Figure 2(c) is a cross-section image of another type of process weak point that causes metal bridging in layer M4 which sits on top of large area without any metal patterns in between M1 and M3.

## HOTSPOT RULES AND RULE BASED PATTERN SEARCH

After determining the hotspot patterns for the known defects, it is important to understand the polygon interaction that causes the defect on the wafer. Process weak points could be a result of interaction from multiple process layers. As examples in the case 2(a) and 2(b) shown in previous section, they are combination of factors that contributed to the defect occurrence: neighboring metal line width, the space between adjacent metal lines, via size and enclosure space, occurrence of Via as pair on neighboring metal lines, and orientation of the two via pairs. All these restrictions of defect pattern element can be captured by the GUI based Anchor Pattern Rule Editor (PRE) tool, as shown in Figure 3 below.

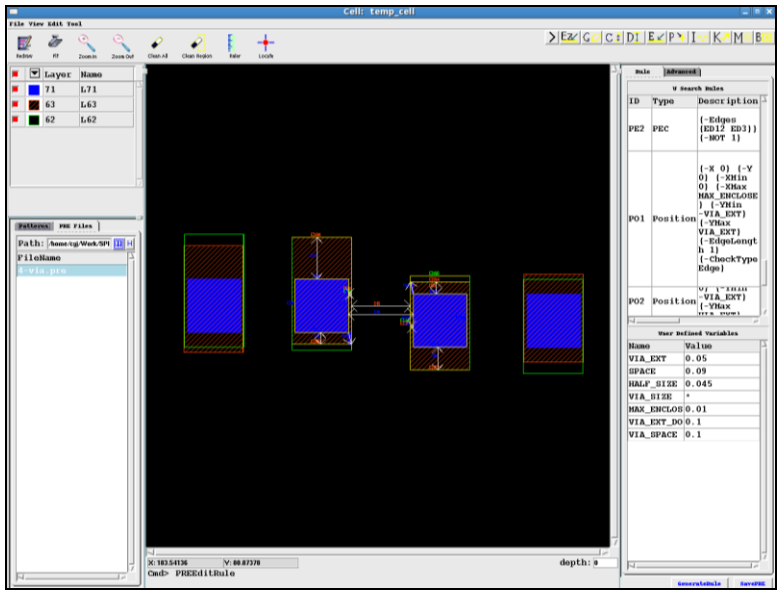



*Figure 3: Hotspot Pattern Rule Generation using PRE--4-via rule for Via induced Metal bridge*

The hotspot pattern rules for space and line width dimensions of via and metal polygons are defined and saved in a parameter rule file, the rule generation time for the *4-via rule* was 10minutes each for 55nm and 65nm designs using the PRE tool. Likewise, hotspot rule files are generated for other known defects. In case the layout cannot be located or generated for a given defect then an expert user can still generate these hotspot rules to define the layout interaction that causes the defect. Each set of rules contain definition of all necessary restrictions in hotspot pattern rule files. With rule file and full chip design as input – a rule based pattern search engine checks the full chip design for any pattern that matches the rule file description. An error mark is placed at the design location where any match is found, as shown in Figure 4. For the 55nm device design 211 hotspot match were found in 2minutes, while 2089 hotspot match were found in 65nm device in 5minutes runtime.

(a) *55nm device* *(b) 65nm device*

*Figure 4: Full Chip view of pattern search result*

## OPTIMIZED CARE AREA INSPECTION

For any wafer inspection Care Area region needs to be defined during inspection recipe setup. Care Area is the region in a die where inspection is carried out and other regions outside Care Area are ignored by the inspection machine. Full dice inspection is generally not used because of long runtime and large number of do not care defects in the result. Effort is made to draw Care Area around critical regions which affect the device performance. Optimization of Care Area is becoming a critical and challenging step in inspection recipe setup for latest designs owing to reducing feature size and increasing complexity. Previous studies have been carried out to use design analysis to classify critical and non critical regions and optimize the inspection regions [4].

The pattern search result locations on full chip indicate the potential hotspots on wafer. Care Area can be automatically generated around these hotspots for optical inspection. Generally the Care Area setup is done manually in fab based on the user experience and guideline by the process engineers. This input of hotspot locations enables faster and efficient recipe setup. Based on the tool limitation of maximum number of Care Area handling, the pattern search result is fed to the inspection machine directly. In Figure 5 is shown the care areas generated using the pattern search result.

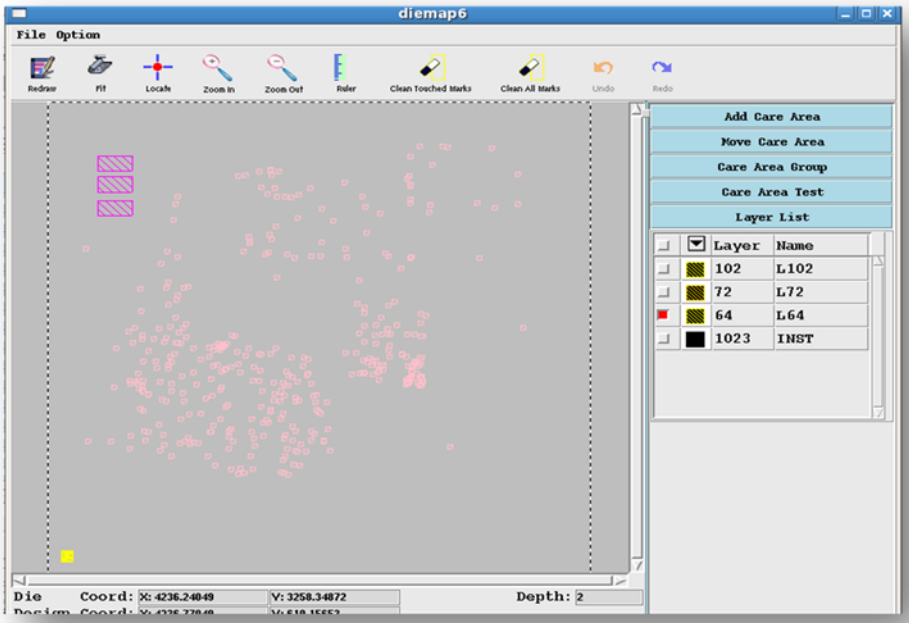



*Figure 5: Anchor Care Area generation around hotspots for the 65nm device*

Optimized Care Area allows to setup high sensitivity inspection recipe on wafer to enhance inspection and detection efficiency. Each hotspot pattern search result is fed to separate Test setup in the recipe. This allows customized threshold settings for each Test to detect particular pattern defect.

## WAFER INSPECTION RESULTS

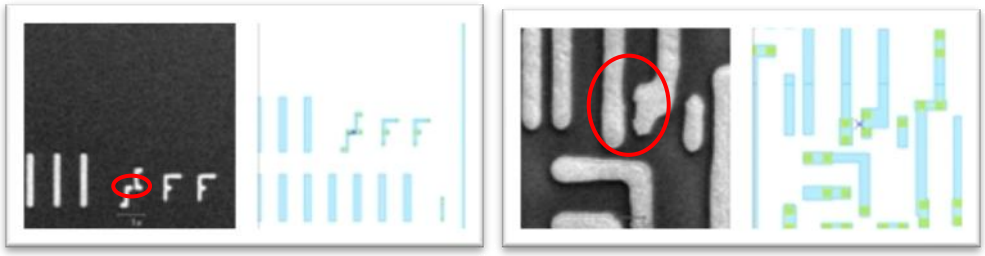
The optimized care area inspection was carried out on PWQ wafers processed using both 55nm and 65nm technologies and the result was correlated with the hotspot pattern search results. The correlation result is summarized in Table 1. 16 out of 23 and 112 out of 262 defects correlated with the pattern search results indicated high probability of potential missing defects, due to process marginality. The PWQ wafer was chosen for this study since the pattern dependent systematic defects are amplified and easy to observe on this wafer by slight variation of process conditions. The inspection plan included the dies marginally close to the device process window.

| Device | Pattern search count | Care Area count | Defect count on PWQ wafer | Correlation with pattern search location |
|---|---|---|---|---|
| 55nm | 211 | 211 | 23 | 16 |
| 65nm | 2938 | 1000 | 262 | 112 |

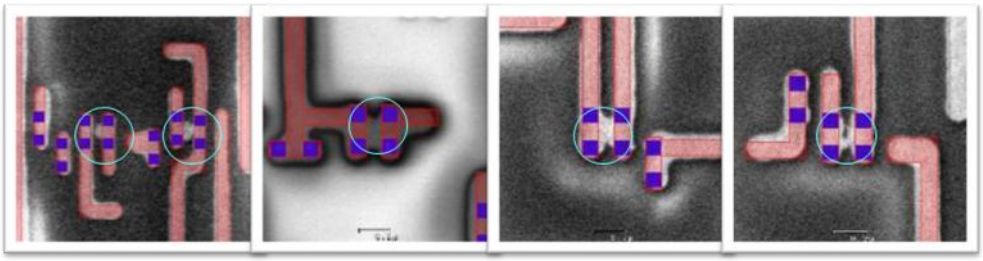
*Table 1: Summary of defect correlation with design for 4-via rule check*

Some critical defects with same signature at new locations were captured guided by rule based pattern search result. Some examples are shown in Figure 6 where the process weak points are superimposed by the layouts. Those defects normally are

hidden in the best process condition and appear with small process variations and impact product yield, as the result. The newly developed approach can easily pick them out and save them in the library. The knowledge in the library can be the guide for future design and process improvements.



(a) *New found defects from 55nm device on PWQ wafer*



(b) New found *defects from 65nm device on PWQ wafer*

*Figure 6: Defect to design correlation for the new found via induced metal bridge on PWQ wafer using the 4-via rule pattern search*

## CONCLUSION

The methodology to detect hidden, yield impact systematic defects using known wafer defects as templates has been developed and demonstrated in this paper. Full chip pattern search was performed for the known hotspots and Care Area was automatically generated around those locations for wafer inspection recipe. PWQ wafer inspection revealed new dice locations with process weak points with minimal process variations. This approach can also be used to feed the critical defect information from one checkpoint to another in order to monitor design [5], or build more robust inspection recipe for other tools. The design information is appropriately utilized to bridge the knowledge gap among different operation teams thereby improving the overall efficiency. Once the hotspot is defined then the fab user can easily utilize the feedback care area information to improve the wafer inspection recipe. Further study is planned to utilize other DFM information for detecting process window and yield limiters.

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