Improvement on OPC completeness through pre-OPC hot spot detection and fix

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ABSTRACT

Design For Manufacturing (DFM) has been paid attention as the feature size on chip goes down below the k1 factor of 0.25. Lots of DFM related ideas have been come up, tried, and some of them adopted for wider process window and as a result, higher yield. As the minimum features are getting shrunk, the design rules become more complicated, but still not good enough to describe the complexity and limitation of certain patterns that imposes narrow process window, or even failure of device. Thus, it becomes essential to identify, correct, or remove the litho-unfriendly patterns (more widely called as hot spots), before OPC. One of the efforts is to write a DFM rules in addition to conventional DRC rules.
In this study, we use the software, called YAM (Yield Analysis Module) to detect hot spots on pre-OPC layouts. Conventional DRC-based search is not able to surpass YAM, as it enables to identify hot spots in either much easier way or even ones that are unable to be found by DRC. We have developed a sophisticated methodology to detect and fix OPC- and/or litho-unfriendly patterns. It is confirmed to enlarge process window and the degree of freedom on OPC work.

Key words: OPC, DFM, process window, design rule, YAM, DRC

Introduction

Design for manufacturing (DFM) has become an important focusing item in the semiconductor industry. Consequently many new DFM applications have arisen and are being widely accepted as one of the key factors in lithography and Optical Proximity Correction (OPC) technology. As semiconductor technology has advanced, design rules of Integrated Circuit(IC) are more and more complicated than before. Therefore some patterns that are still within the design rules have narrow lithography process margin, especially 2-dimensional pattern[1]. DFM rule goes beyond the traditional design rule check (DRC) and offers additional check items and recommendations to ensure lithography-friendly and OPC-friendly designs. In addition it is possible not only to improve process margin but also to achieve better yield by modifying circuit design. The most critical yield loss will be related with systematic defects such as design and

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lithography process issues sub-90nm technology. Figure 1 illustrates the yield trends at technology nodes and the causes of yield loss. As see in figure 1 random defects are no longer the dominant yield loss mechanism, only design can provide some solutions to relieve lots of burdens due to the smaller size effect and the adoption of very low K1 process. In this paper, we used Yield Analysis Module (YAM) tool before running OPC to optimize layout. YAM can check lithography unfriendly and OPC unfriendly pattern (hot spot) by rule based method, while those patterns can not be detected by DRC.

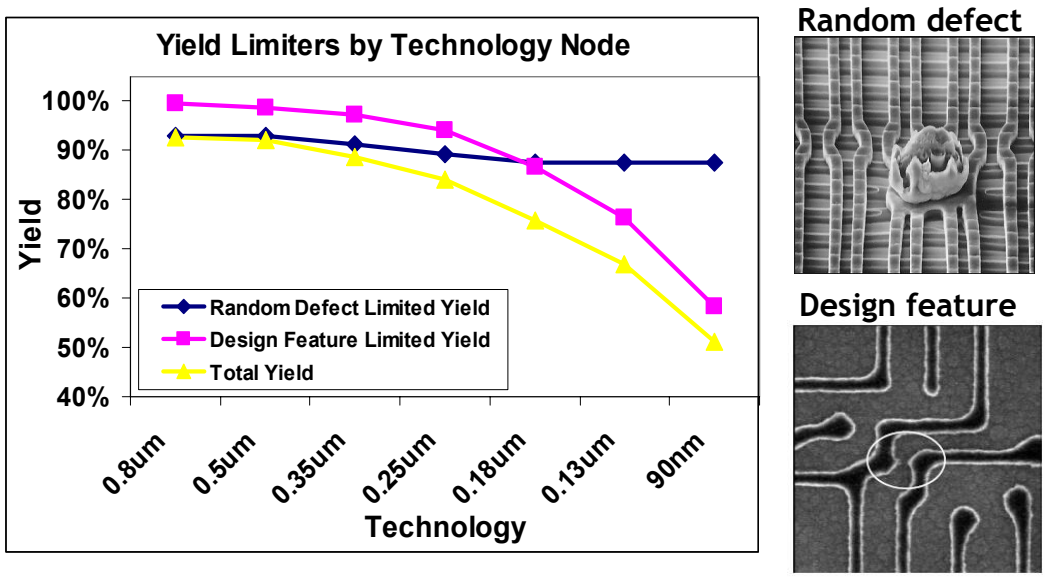

Figure 1. Yield trend at technology (Figure extract from PDF solutions Inc., 2006)

Suggestion of new design flow with hot spot checking

As mentioned in the previous section, in low-k1 lithography, hot spots appear frequently in the case of using conventional design methodology[2]. YAM has wide range of applications in DFM, from design phase (check OPC unfriendly patterns and litho unfriendly patterns using rule base), to manufacturing space before running OPC. There are lots of commands in YAM to search hot spots. Following figure 2 is show the example of YAM analysis.

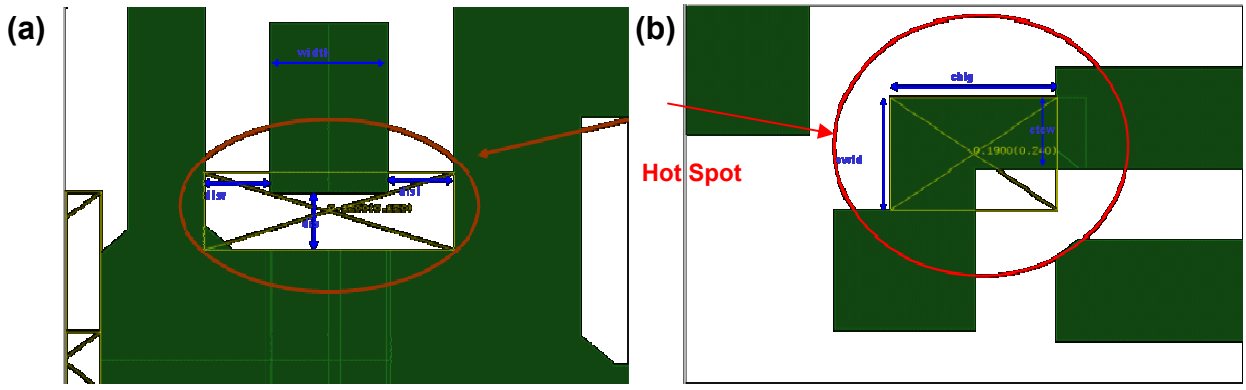

Figure 2. Example of YAM analysis (a): check line end on metal or poly whose length and/or width and/or spacing meet the spec. (b): check small connecting segments (corner crack).

Figure 3 illustrates new process flow in design and manufacturing, using YAM. At the normal design flow if we can't detect hot spot area at the layout drawing step, we will find out hot spots after verification step. However design modification after verification step have a bad influence on development Turn Around Time(TAT)[3, 4, 5]. So, we suggested new design flow considering hot spot management at the early stage of development. In this new design flow, YAM running is performed to fixing hot spots before DRC/MDP step. Designers can find out hot spots in YAM running results, then they can modify layout before OPC running. We save the TAT using this method.

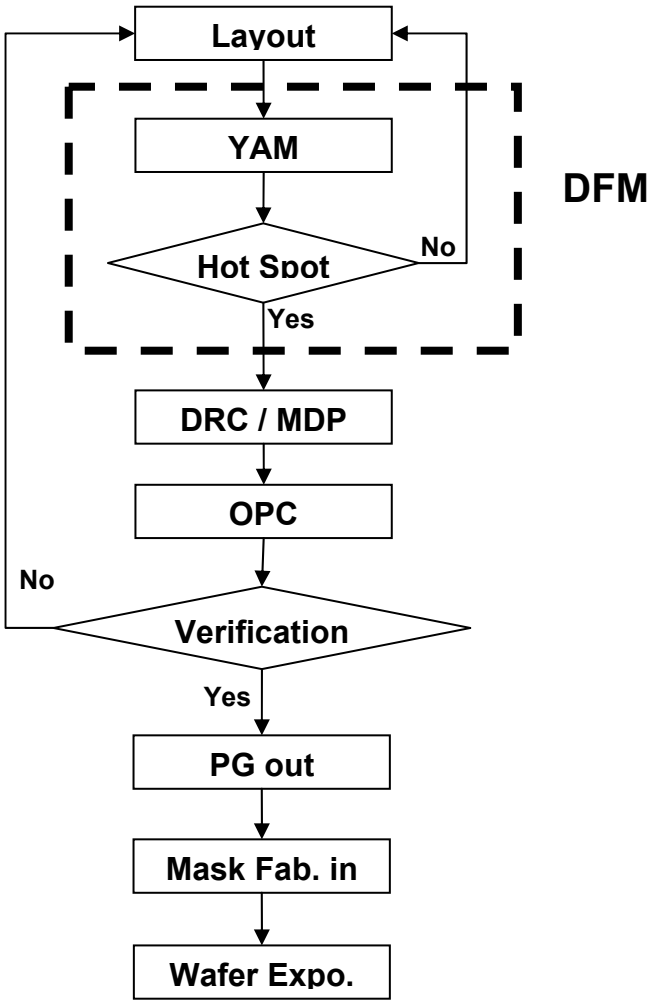

Figure 3. Design flow with hot spot fixing using YAM.

Experimental

We will compare two different sets of simulation and wafer data. One is data with poor process margin resulted from worse design, and the other is data with improved process margin by design optimization. For obtain process margin data, we applied the new design flow to poly layer which is most critical layer.
Scanner conditions were fixed at NA 0.60 and annular illumination of 0.85 outer and 0.45 inner. And 6% transmission of attenuated Phase Shift Mask(HTPSM) was used. The test reticle has various test patterns contain for estimate process

margin and various hot spots. Many hot spots were split from tight design to loose design. Figure 4 shows the example of various hot spot split items. Line and space are split from restricted design rule to arrow directions by 0.01 μm steps. We measured process margin data of all split patterns to catch the reasonable specifications of each pattern.

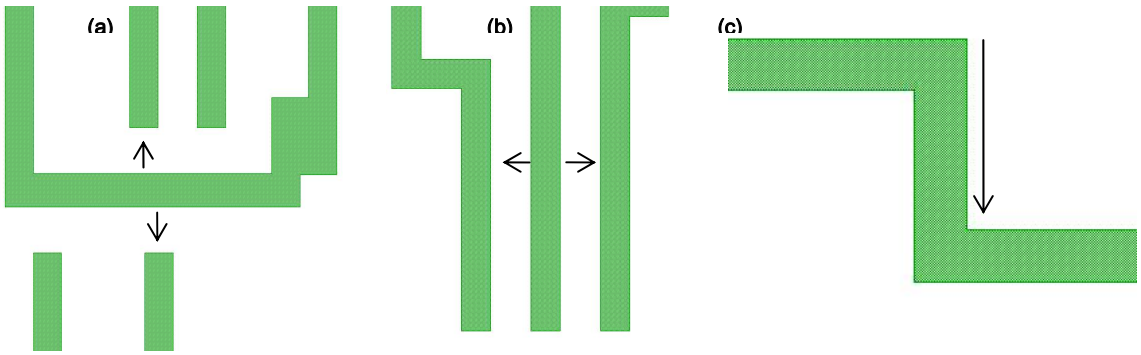

Figure 4. Test pattern split items on test reticle

Result and Discussion

Table 1 shows number of hot spot and hot spot fixing rate of mimic-logic test block. For this test block, hot spot fixing rates of poly layer are from 50% to 100% for each hot spot group.

	Hot Spot	# of hot spot	Modification rate
	LINE_END_CHECK	13	100%
	3_LINE_CHECK	348	100%
	CORNER_CRACK_CHECK	6	50%
	CORNER_JOG_CHECK	35	55.6%
	CORNER_NOTCH_CHECK	34	83.3%

Table 1. Hot spot modify rate after YAM running for poly layer

LINE_END and 3_LINE which are most critical hot spot patterns are fixed 100%. Moreover crack, jog and notch which are minor hot spot patterns are fixed 50%, 55.6% and 83.3% respectively. Some patterns cannot be fixed because of

design rule restriction, contact coverage and so on. However as you can see in this result, most of hot spots are fixed at the early stage of development using YAM running result.
Figure 5 shows the simulation results of comparison with original layout and fixed hot spot layout about LINE_END_CHECK. The most inside line of figure is the simulated contour of resist image under over-dose error. As shown in figure 5, in original layout there is no lithographic margin at the point of hot spot. After fixing of space size by upward, simulation image of hot spot is improved. Wafer results for the same layout are shown in figure 6. Both of the original and fixed hot spot patterns are exposed on wafer under best dose condition and best focus condition. These images show the same result with simulation results, in original layout there is no lithographic margin at the point of hot spot. Figure 7 shows SEM image compares focus exposure matrix of original layout with fixed layout. Dose condition was split from -4% to +12% at best condition and focus condition was split from -15% to +5% at best condition. For original pattern, in under dose condition below -4% and in under focus condition below -10%, most of the resist images are deformed. However for fixed pattern, even in under dose condition and under focus condition, most of the resist images are form correctly. It means process window is expanded.

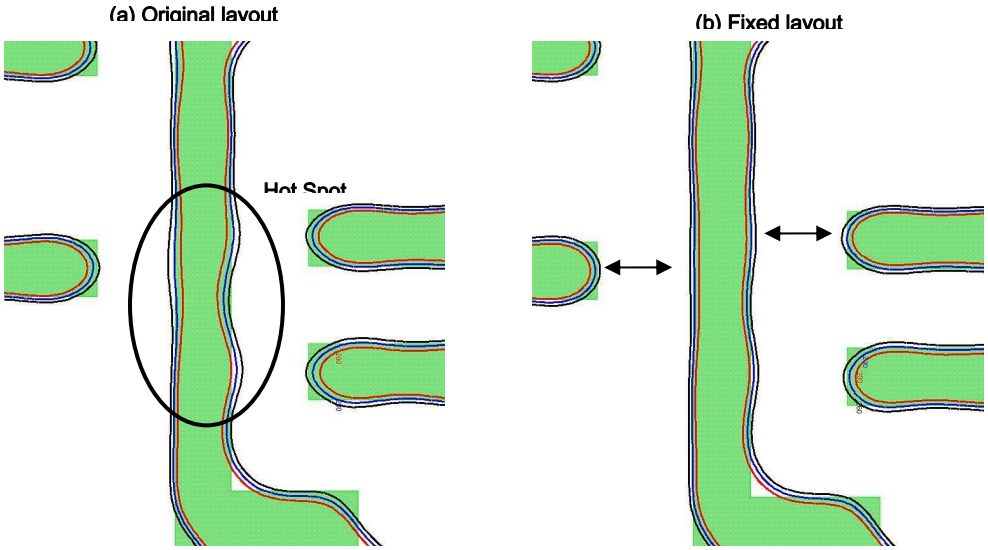

Figure 5. Simulation results of comparison with original layout and fixed hot spot layout

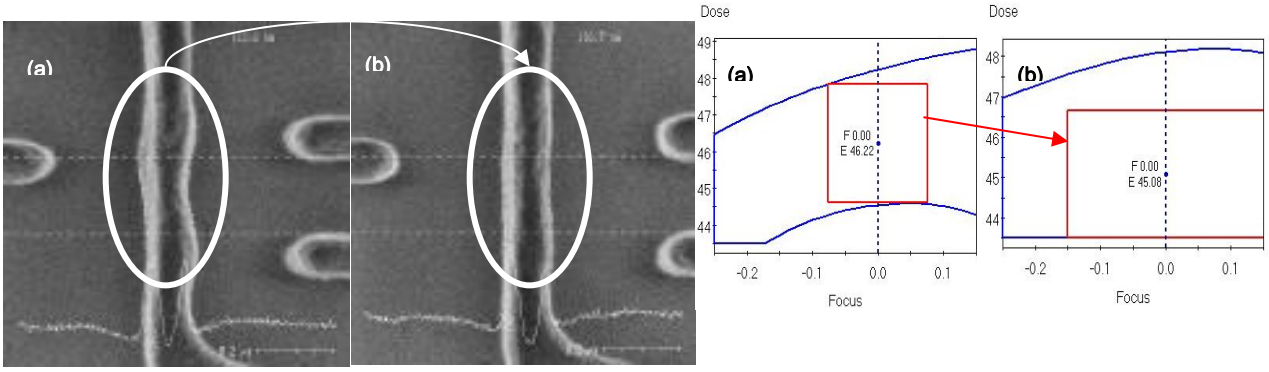

Figure 6. (a)Original layout, (b)Fixed layout.
Wafer result and process margin comparison with original layout and fixed hot spot layout

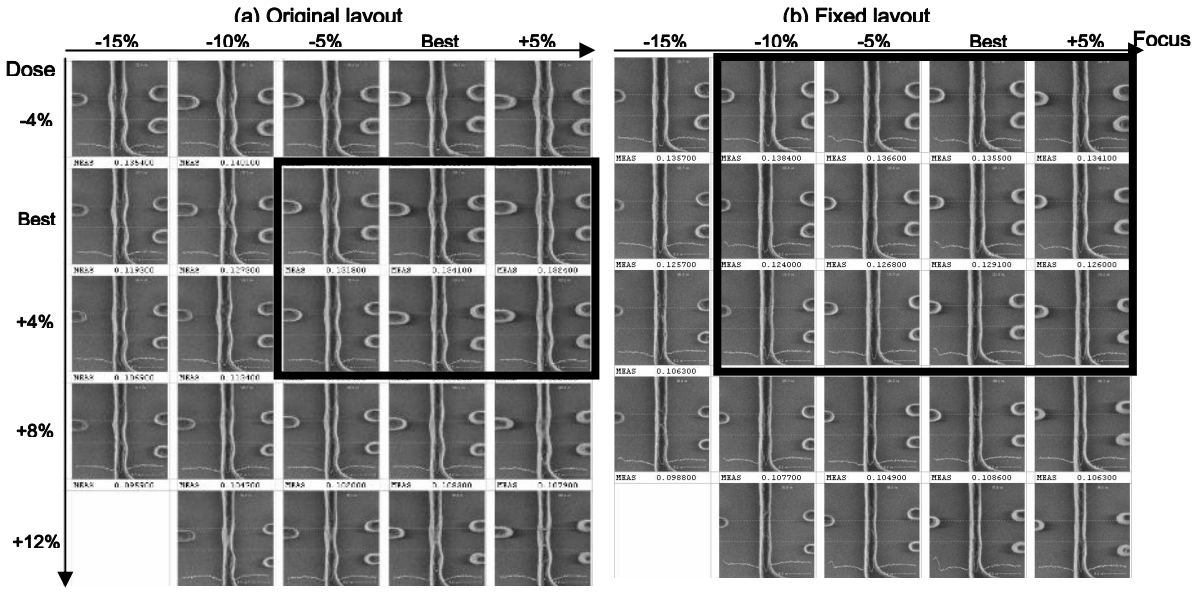

Figure 7. SEM image of dose focus matrix indicating lithography process margin

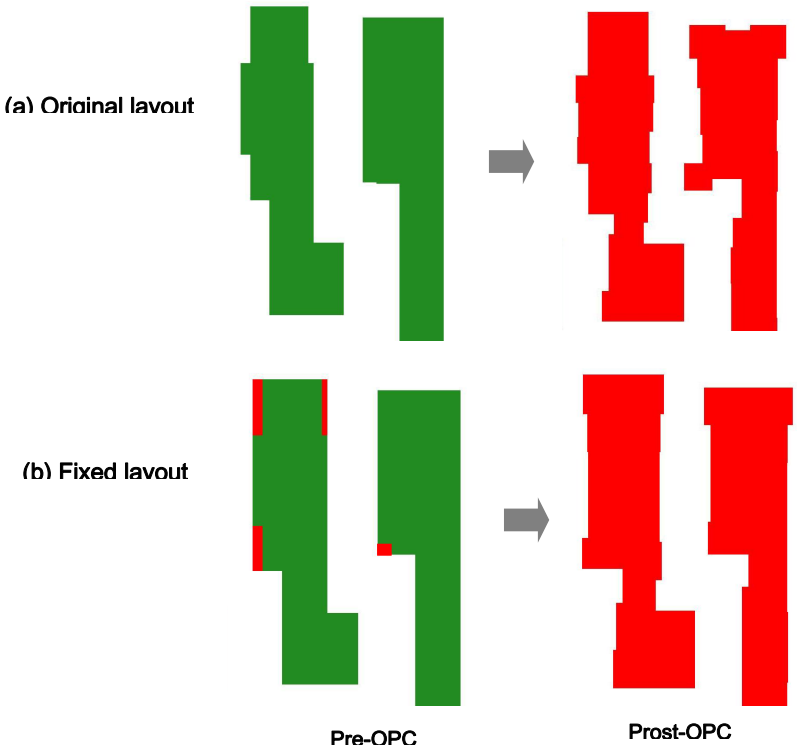

Figure 8. Result of abnormal OPC caused by corner_notch

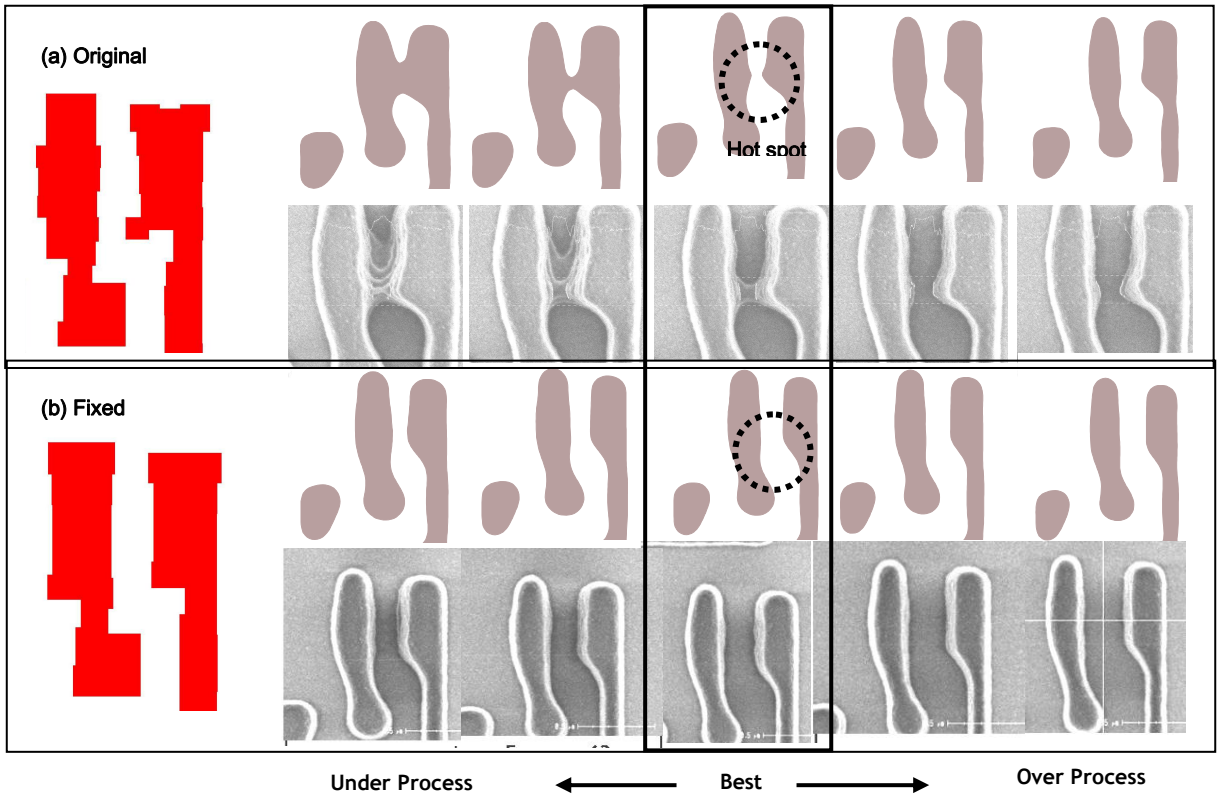

figure 9. OPC & Wafer patterning results of original layout and fixed layout

The examples of fixing small cracks, jogs and notches in original design are followed. We can call them as OPC-unfriendly patterns since they create unnecessarily complicated OPC patterns. They make many errors after OPC because OPC model recognizes just as one of small features that it should care. This generates many false alarms at OPC verification and mask rule check[6]. Figure 8 shows the result of abnormal OPC caused by corner_notch. As expected, the logic layout gets more cleaned OPC result in terms of modified corner_notch by hot spot fixing.
As shown in figure 9, the lithographic process window is significantly improved: due to corner_notch the OPC result has been aggressive and it results in bridging at wafer. As a comparison, post-OPC layout using fixed layout application is simpler than the original one and wafer process with fixed layout becomes more stable against the process variation.

Conclusion

Sub-90nm technology process had more complicated design rules than the previous process technology. Sub-90nm technology lithography causes the situation that hot spots appear frequently. To overcome hot spot issues under low-k_1 lithography condition, the new DFM scheme with the YAM running and hot spot fixing flow was developed. Suggested new design flow considering hot spot management at the early stage of development. In this new design flow, DRC/MDP followed by YAM running is performed. Designers can find out hot spots in YAM running results, then they can modify layout before OPC running. We save the development TAT using this method.

In this study, several hot spots were confirmed at wafer stage. In original layout there is no lithographic margin at the portion of many hot spots but for fixed pattern, most of the resist images are form correctly. It means process window is expanded.
Finally the new DFM scheme with YAM running and hot spot fixing was applied on a local test block. After fixing, a number of hot spots are reduced about 65%. This result was very bright prospect, therefore, this newly developed DFM scheme is going to be very effective for application at 90nm node and beyond.

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