Design for Manufacturability Guideline Development: Integrated Foundry Approach

Hyesung Lee[a], Yeon-Ah Shim[a], Jae-Young Choi[a], Kwang-Seon Choi[a];
Joanne Wu[b], Bo su[b], Xinwei Zhou[b], and Kenny Kim[c]

[a] DongbuHiTek, Sanwoo-Ri, Gamgok-Myeon, Eumseong-Gun, Chungbuk, 369-852, Korea;
[b]Anchor Semiconductor, Inc.5403 Betsy Ross Drive Santa Clara, CA 95054 USA;
[c]International Technology Alliances, Inc.,P.O. Box 641181, San Jose, CA 95164-1181 U.S.A

Abstract

It has been widely accepted that to ensure good yield in IC wafer manufacturing, early adaptation of DFM (Design for Manufacturability) guidelines in design phase is required and it is particularly true in Foundry business. Integrated foundry approaches for DFM guideline development were presented in this paper. With emphasis of process variations and process sensitivity impact on design patterns, we describe the procedure of the combination of rule-based and simulation-based lithographical hotspot pattern characterizations. An evaluation of process sensitivity metrics for analyzing potential pattern hotspots is then described. In addition, based on hotspot pattern severity, repeated patterns from different designs are saved into a pattern library as knowledge deposition tool and those patterns can be easily identified later in new designs through pattern search, which is much faster than simulation based hotspot detections. With this approach, a set of DFM compliance rules is derived to designs in the design implementation stage for both 110nm and 90nm technology nodes, striving to gain more yield, device performance, and improve time-to-volume production.

Keywords: DFM(Design for Manufacturability), Simulation based hot spot detecting, DMF pattern library, Scoring index, hot spot fixing

1. INTRODUCTION

As fabrication technology advances towards deep sub-wavelength lithography domain, two dominant trends make wafer manufacturing more and more difficult. The first, RET (resolution enhancement techniques) /OPC (optical proximity correction) becomes more and more complicated and complex, as result, fractured mask data size and associated mask making costs due to longer writing and inspection time have also been increased drastically. Rule-based DFM(design for manufacturability) guidelines target to reduce and remove unnecessary jogs, notches and extra vertex in designs, which in turn, will reduce RET/OPC complexity and ultimately mask making costs. The second, process window becomes smaller and smaller with fixed exposure wavelength. Simulation based lithographic hotspot pattern detection and characterization is necessary for decreasing process windows. Because rather long OPC decoration time due to increased complexity of OPC, simulation based hotspot detection method is desirable even before OPC decoration. Moreover, in terms of time consuming DFM is quite well known application method for both design and manufacturing. If we tape out the DB (data base) without DFM, the time to complete the IP development or yield-up takes quite much than in case of taping out with DFM. As a result, the cost is also much higher. For these reasons, many efforts have been making by designers as well as OPC engineer.

Recently, as it is shown in the figure 1 there are three main approaches to apply DFM to our general procedure of chip making which is from design to silicon process. The first, simply, we can add many rules in existing design rules. Thus, design rules are getting complex with more restrictions or rules. Then the design for yield is also well known field with reducing random defects effects on yield of device. Lastly, there are design and layout verification, and OPC which are carried out by designers or OPC engineers. Advantage of this last approach is the time to apply is quite early in general DB flow. Especially, in this paper it is going to be talked about the LFD (litho friendly design) in the view point of OPC engineer. So far, there are two main approaches to detect defective patterns, those are rule based pattern searching and

Photomask Technology 2008, edited by Hiroichi Kawahira, Larry S. Zurbrick,
Proc. of SPIE Vol. 7122, 712221 · © 2008 SPIE · CCC code: 0277-786X/08/$18 · doi: 10.1117/12.801421

simulation based pattern searching. Although, rule based pattern searching is simple and powerful way of application to flow, there are several limitations which will be followed. First of all, we can find only currently recognized hot spots. Then, it's getting hard to define complex patterns. Finally, we can build the rules after completing silicon process. Thus in order to complement the rule based pattern searching, we trust simulation based pattern searching will be useful.

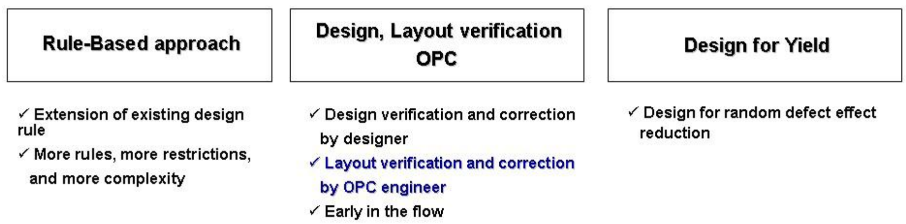


Fig. 1. Recent main approached to DFM and those characteristics

1.1 How DongbuHiTek develop the DFM guideline?

For the first phase of our DFM in this study, rule based pattern searching had been used for find or define hot spots, then, from the results of rule based hot spot searching, DPL (DFM pattern library) had been built as it is described in figure 2. Then it is found out that pattern missing could be happening or the results of pattern searching are too much to review at one time due to the limitation of rules. Thus, in order to reduce the defective pattern review scope and to find potential hot spots simulation based pattern searching has been studied based on the DFP (design for patterning) simulation.

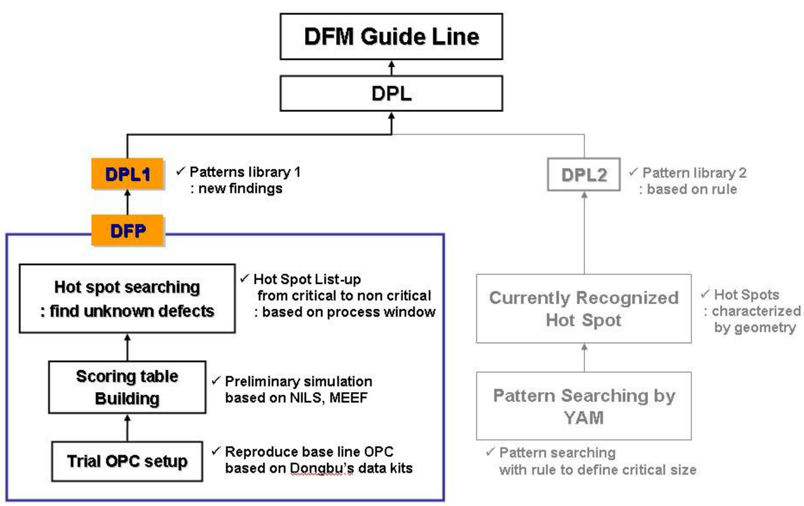


Fig. 2. DFM guideline building flow, based on simulation searching (left), based on rule searching (right)

1.2 What the DFP is?

As we can see in figure 3 there is simple introduction of DFP what it is used for simulation for DFM. With initial DBs, so-called trial OPC was made, with our process data kit. This trial OPC will be descried later in detail. Based on the trial OPC results, defective pattern searching is conducted. In this stage, we can list up the hot spots in order of risk. This hot spot list is based on the process window such as NILS, MEEF, or defocus. As a result of PW (process window) aware simulation, the new hot spot will be saved as pattern library or DB will just take their own flow. DFP can control the all the procedures from simple litho simulation, searching defective patterns, to saving patterns to DPL (DFM pattern library).

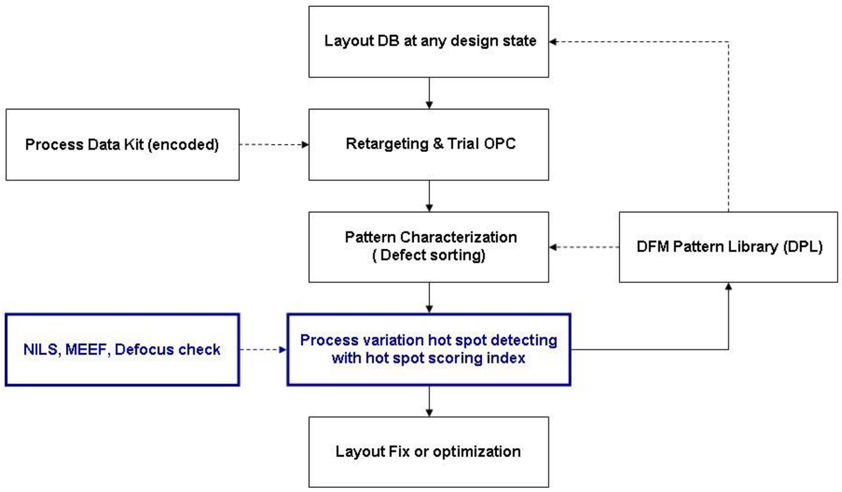
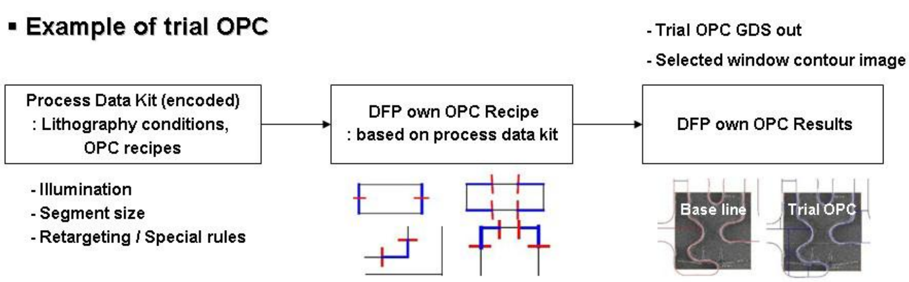


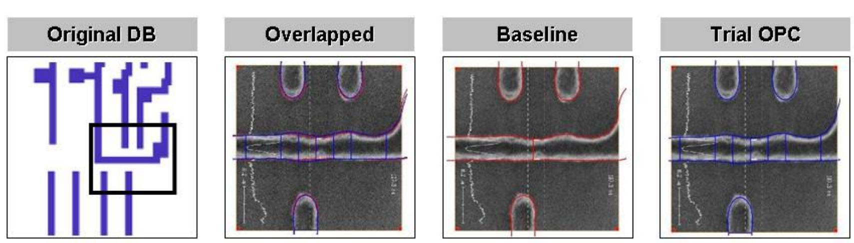
Fig. 3. Simple description of DFP procedure

2. RESULTS OF TRIAL OPC BY DFP

In order to restore baseline OPC which means dongbuhitek's own OPC results, we prepare process data kit including lithography process conditions, OPC recipes such as segment size, retargeting rule and so on. These data then put in DFP recipe. After complete recipes, DFP shows the trial OPC results as GDS format, then, it is possible to see the contour images at the selected area. The detailed process of trial OPC is described well in figure 4. After many trials and errors, finally the initial version of trial OPC was fixed. There are also an example results of trial OPC in figure 4.



(a) Detailed process of trial OPC



(b) Contour results of trial OPC

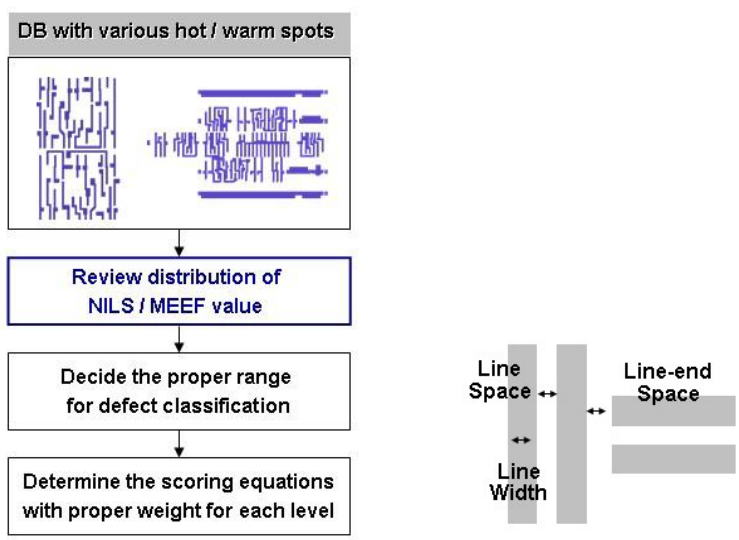
Fig 4. Description of trial OPC

As you can also see in this figure 4, with this given gds, first the trial OPC was executed then, the contour image was compared with base line contour image. As it is shown in SEM overlapped images, the blue contour image from trial OPC is well matched with red contour image which is of baseline and wafer image of this weak point.

3. RESULTS OF DFP SIMULATION

3.1 Basic concept and flow

In figure 5 the whole process of DFP simulation is explained. After we finalize DFP trial OPC recipe, DFP process window simulation based on the NILS, MEEF or Defocus model was conducted to define the risk index for each range. In this step, firstly, we've tried to check process variation with NILS and MEEF parameter only. It is because defocus model should be very accurate to give accurate standards however, the defocus model is still under developing. Then during the simulation, it is able to find the features for instance, space adjacent to line, line width and space between line end as those are in figure 5. For this simulation, it is expecting to find the unknown hot spots, and reduce the hot spot review scope by the hot spot list by risky index. Then, finally, reorganize currently recognized hot spots to be aware of its degree of risk. Actually, it is not for the detailed litho characteristic simulation therefore, we've tried to list up the patterns simply dependant on the value of NILS and MEEF itself. The results of these simulation is shown in the next session 3.2.



(a) Simulation procedure (b) Examples of simulation feature

Fig 5 Basic flow of DFP simulation

3.2 Simulation results

After complete the simulation with DFP, user can see the counts of defective patterns for the each value of NILS or MEEF. As generally known of, the patterns which have small NILS value those are located at the left side of the graph in figure 6 can be considered the higher risky pattern. Then MEEF distribution is also shown the other side of the figure 6. In case of MEEF, the patterns put on the right side of the graph can be hot spots. Since we have to review lots of case to define as hot spots, we're intentionally use DB including many defective patterns which are used to be known as critical hot spots for NILS, and MEEF simulation. Then sort those hot spots by the location at the distribution they have. Accordingly it is divided the proper range to define risk level of hot spots based on the currently recognized patterns in the DB.

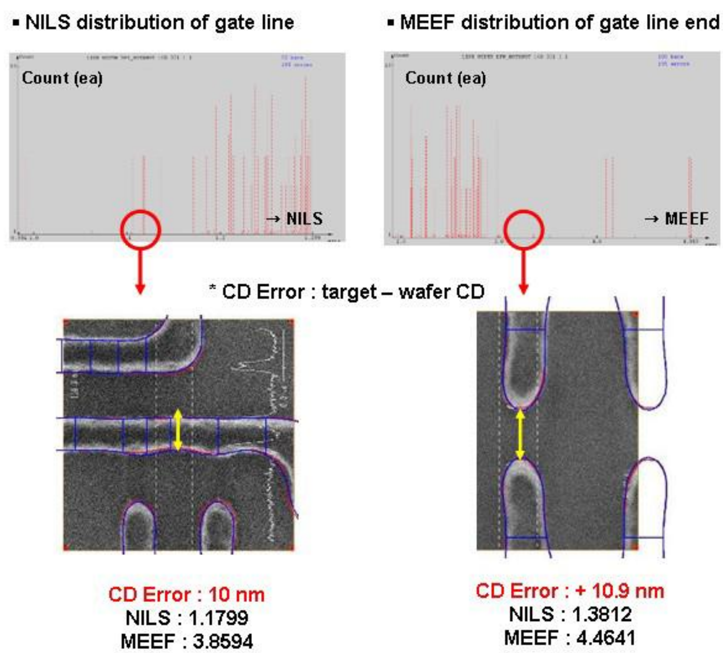


Fig 6. Simulation results of DFP in case of line width with NILS (left) and line end space with MEEF (right)

3.3 Hot spot scoring results

Based on the previously shown data, hot spot scoring index has just fixed as shown in figure 7. These results are listed up based on the condense expression as below in exp (1). This result in figure 7 is in case of gate line width and in this case the score varied from 1.6 to 32.8. As it is reviewed the patterns in the graph, most of patterns are properly positioned, except for several patterns. However, after many trials and errors, the false errors are getting reduced a lot. Moreover, in order to make the influence of both NILS and MEEF balanced, we try to employ many different values for weight in expression (1), then determine proper value for each range.

$$Score = weight \times f(NILS) + weight \times f(MEEF) \qquad (1)$$

As it is shown in figure 7, the pattern located at the left has the score as 1.68, this pattern was confirmed as least risky on wafer also. Furthermore, the pattern which has score value of 15.32 is also confirmed on wafer as non risk pattern. Thus, we can use this scoring system to sort patterns then if the patterns in hot spot group have the score value below 15, those patterns can be filtered out from the hot spot group.

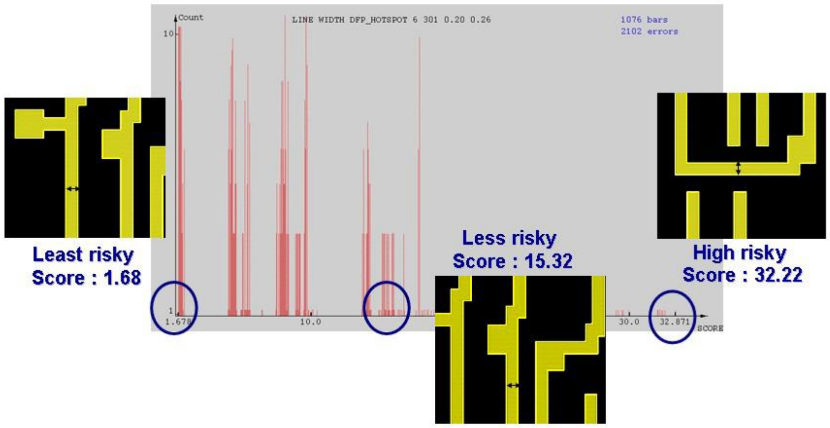
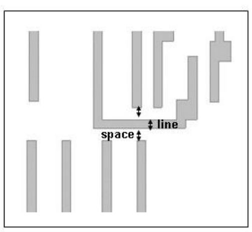


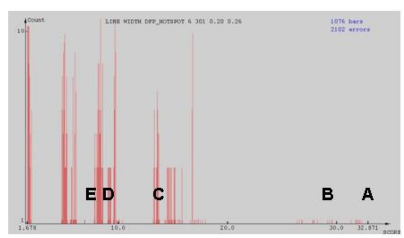
Fig 7. Hot spot scoring results based on the DFP simulation with NILS, MEEF

3.4 Process window confirmation

Data of figure 8 is PW confirmation on wafer and hot spot scoring results in given patterns. In this case the pattern can be risky for both pinching and bridging, we split the space size between line end T-junction to release the risk. Start from minimum design size of A, the space of both side of the line is increased. As you can see the SEM images and DoF margin at the table, when the space size becomes larger, CD error and DoF margin of the line getting improved. Thus patterns which have the space size of D and E, can be considered warm or sweet spots. Moreover, if we need, we can filter out the patterns which have less score than D or E from the review report. That must reduce the time to review the hot spot or the size which is D or E can be recommended as the DFM guideline size for this structure.



Space CD	Score sum
A	32.22
B	29.13
C	17.04
D	9.89
E	9.52



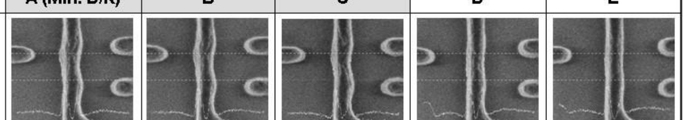
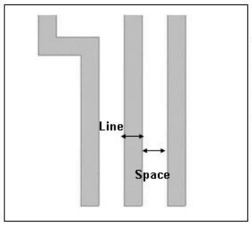
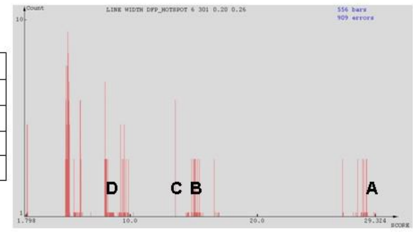
Space CD	A (Min. D/R)	B	C	D	E
Target Image					
CD Error @ best focus	+ 2.1 nm	-1.5 nm	0 nm	0 nm	-0.9 nm
DOF@EL 8%	-	-	0.14 um	0.30 um	0.30 um

Fig 8. Hot spot searching and wafer confirmation to verify risk index (line end T-junction)

For this case of triple lines I figure 9, the line at the middle seems to be narrower than the others. Moreover, it used to be considered as poor marginal patterns so far in particular at the minimum design rule size of space. Accordingly, space between line outside was split from min, design size. As we can observe from the hot spot sore graph, The poor marginal pattern of A is located at the high risk region. Then the pattern of D is located at the less risk region.



Space CD	Score sum
A	29.27
B	16.86
C	15.09
D	9.56



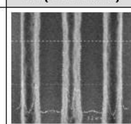
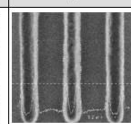
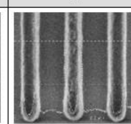
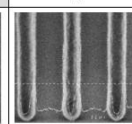
Space CD	A (Min. D/R)	B	C	D
Target Image				
CD Error @ best focus	+ 2.1 nm	-3.7 nm	-0.3 nm	-0.6 nm
DOF@EL 8%	-	-	0.14 um	0.30 um

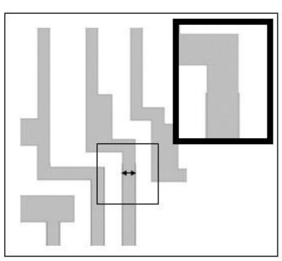
Fig 9. Hot spot searching and wafer confirmation to verify risk index (triple line)

3.5 Hot spot searching

With initially fixed scoring index hot spot searching was carried out on newly taped out DB. Influenced by large MEEF at the indicated line on the left gds figure in figure 10, the score seems quite high enough to consider this pattern as hot spot. After checking with hot spot scoring system, wafer confirmation was also followed consequently. As we can see through the table on right top, the pattern shows large CD error of 8 nm at the process center condition. Moreover, DoF margin was also too poor to ignore.

CD Error	NILS	MEEF	Score sum
- 8.0 nm	1.15	3.24	**28**

▪ **Real chip simulation results with DFP**



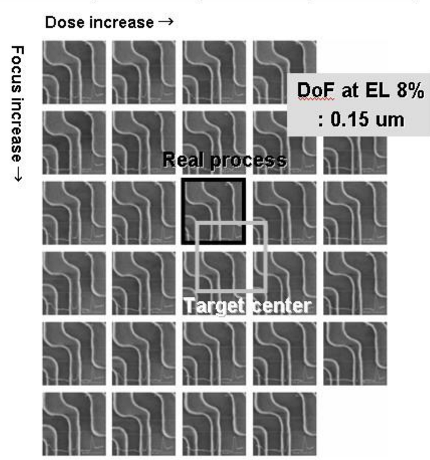
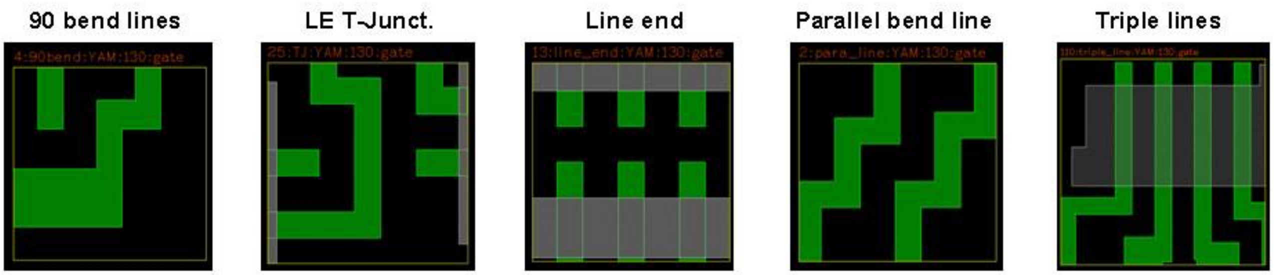


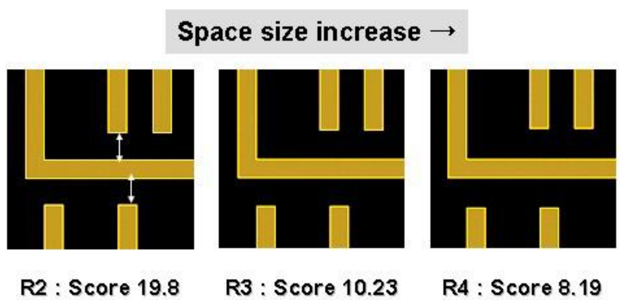
Fig 10. Hot spot searching with newly taped out DB and DoF margin data

4. DFMPATTERN LIBRARY BASED ON DFP

In figure 11 (a) we can see the our currently built DPL by rule based approach. Then after completing the model based pattern searching sequence, it’s been tried to reorganize this pattern library based on the hot spot scoring index. As it is shown on the example images in figure 11 (b), line end T-junction are specified by risky state with their score. Thus, designers possibly check the DB with our system, then characterize those patterns from higher risky to less risky among the results they have on DB. Although this score is not giving absolute standard for sorting weak points, designer can distinguish the patterns based on the litho simulation results.



(a) DFM pattern library with rule based pattern searching



(b) DFM pattern library with simulation based pattern searching in case of line end T-junction

Fig 11. Hot spot searching with newly taped out DB and DoF margin data

5. CONCLUSION

Figure 12 is our suggestion of DFM flow with model at the stage of design, designers check the hot spot with given data kits which are including foundry process conditions, and OPC recipe. Then analyze hot spot based on the given scoring system. Then if they find critical weak point they revise design in advance to the silicon process or OPC process. Or if it is used by OPC engineer, They can easily find the potential hot spot. Therefore, they can fix or update the recipe before the PG-out. Finally, I’d like to conclude my study. With suggested design development flow in figure 12, we can fix designs or layouts before the silicon process. Accordingly, we can reduce the TAT (turnaround time) to market and time to ramp up the yield. Furthermore, in the view point of OPC engineer, we build PW aware DFM pattern library and find unknown defects and finally it can be used for DB cleaning with clearing OPC unfriendly pattern.

In the end achievements of our study can be summarized first DB flow TAT reduction and faster yield-up and PW aware DFM pattern library building, unknown defects finding then finally DB cleaning with reducing OPC unfriendly patterns.

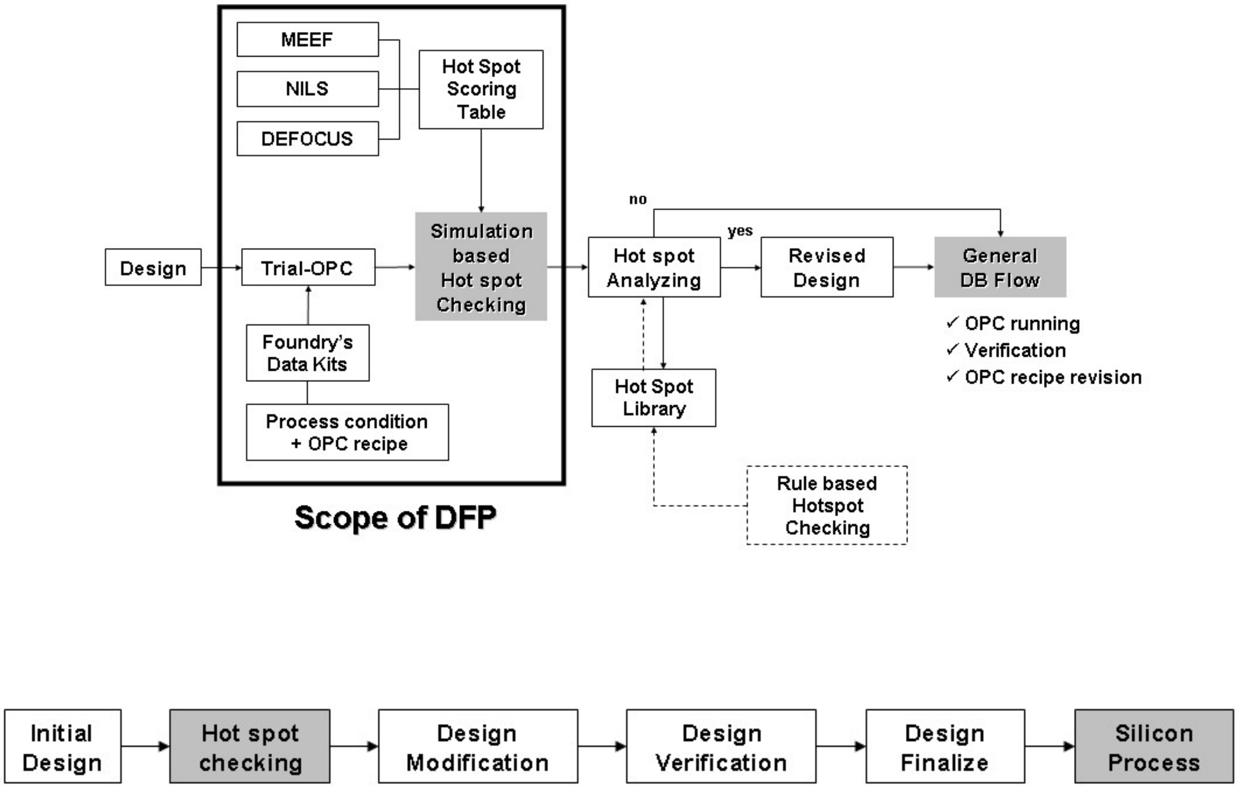


Fig 12. Newly suggested DFM flow in earlier stage

REFERENCES

[1] Yeonah Shim, Jaeyoung Choi, Jeahee Kim, Bo Su, Ping Zhang and Keun-Young Kim, Proc. of SPIE Vol. 6925, 692513, (2008).

[2] Sachiko Kobayashi, Suigen Kyoh, Toshiya Kotani and Soichi Inoue, Proc. of SPIE Vol. 6521, 65210B (2007).

[3] Beom-Seok Seo, Woon-Hyuk Choi, Jong-Woon Park, Sung-Su Woo, and Sung-Ho Lee, Proc. of SPIE Vol. 6521, 65210Y (2007).

[4] Shigeki Nojima, Suigen Kyoh, Shimon Maeda and Soichi Inoue, Proc. of SPIE Vol. 6925, 69250Z (2008).

[5] C.C. Chang, I.C. Shih, J.F. Lin, Y.S. Yen, C.M. Lai, W.C. Huang, R.G. Liu, and Y.C. Ku, Proc. of SPIE Vol. 6925, 69251R (2008).

ACKNOWLEDGEMENT

DongbuHiTek really appreciates both USA and Shanghai Anchor semiconductor's support with devotion and sincere comments on DongbuHiTek's DFM project. In addition, we're giving best thanks for kind support of International Technology Alliance.