Systematic Defect Filtering and Data Analysis Methodology for Design Based Metrology

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ABSTRACT

Recently several Design Based Metrologies (DBMs) are introduced and being in use for wafer verification. The major applications of DBM are OPC accuracy improvement, DFM feed-back through Process Window Qualification (PWQ) and advanced process control. In general, however, the amount of output data from DBM is normally so large that it is very hard to handle the data for valuable feed-back. In case of PWQ, more than thousands of hot spots are detected on a single chip at the edge of process window. So, it takes much time and labor to review and analyze all the hot spots detected at PWQ. Design-related systematic defects, however, will be found repeatedly and if they can be classified into groups, it would be possible to save a lot of time for the analysis.
We have demonstrated an EDA tool which can handle the large amount of output data from DBM by reducing pattern defects to groups. It can classify millions of patterns into less than thousands of pattern groups. It has been evaluated on the analysis of PWQ of metal layer in NAND Flash memory device and random contact hole patterns in a DRAM device.
The result shows that this EDA tool can handle the CD measurement data easily and can save us a lot of time and labor for the analysis. The procedures of systematic defect filtering and data handling using an EDA tool are presented in detail

Key words: Design Based Metrology, EDA tool, Systematic defect filtering

1. DESIGN BASED METROLOGY TOOL

A wide-field pattern inspection system which can compare the pattern on wafer to the design layout has been developed. NGR2100^{TM} can compare the real printing images with designed target layout and measure the CD of all the features in a chip. It consists mainly of two parts, the hardware to acquire wafer images and the software to compare wafer images with CAD layout and analyze the edge placement error. The former is called Electron Image Acquiring System (EIAS) and the latter Geometry Verification Engine (GVE).

The key feature of EIAS is the high-resolution and high-speed secondary electron acquisition capability to acquire images without field distortion over wide scan field. GVE compares the target GDS layout with SEM images acquired at EIAS and detects systematic defects. The systematic defects are classified and grouped according to the geometry or shape of features, and would be put on a DFM and APC platform. Due to the capability to cover the whole chip area with the high-resolution and high-speed, it would be the suitable verification tool for DFM and APC feed-back.

The verification flow using NGR2100^{TM} is illustrated in Figure 1.

1. CAD data are converted into reference geometry
2. The edges of SEM images obtained by EIAS are detected at Edge detector.
3. The image and CAD data are aligned by using the edges and the reference geometry.
4. The geometry verification procedure is then performed based on a bias calculation or CD calculation.

The geometry verification uses a bias, a distance between detected edge and a line of the reference geometry. The bias is calculated pixel-by-pixel and can be compared with the criterion defined by the user.

There are two types of inspection mode in NGR2100^{TM}. One is CGV (Critical Geometry Verification) mode which means 2D GDS SEM and measures all the CD values in the inspection area with high accuracy. CGV mode is used as a verification tool for the hot spots which simulation predicted in MBV step or for the precise CDU analysis of some specific features. The other is RDI (Repeated Defect Inspection) mode which detects repeated defects in a full chip with high throughput. If the distance between detected edge and a line of the reference geometry exceeds a criterion, it is recognized as a defect having edge placement error. With RDI mode, all the systematic defects in a full chip can be identified. So, RDI mode is used as a verification tool for the unpredicted hot spots by simulation.

NGR2100^{TM} has several verifiers to classify pattern features according to the shape and function in the DB. They are line end, corner, space width, line width, Gate on Active – measures Gate width on Active area – and so on. It is even possible to measure the overlay error between the two layers by comparing the centers of the image of each layer.

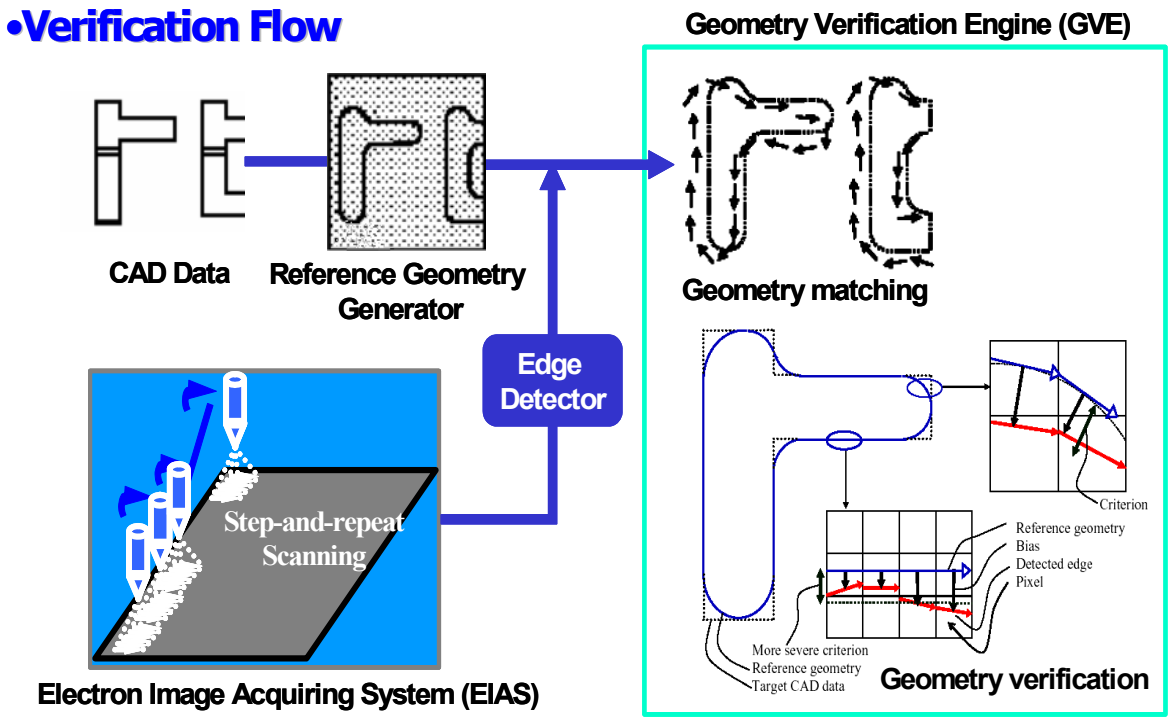

Figure 1. CD Verification flow of NGR2100^{TM}

2. HOTSPOT PATTERN ANALYZER

The Hotspot Pattern Analyzer (HPA) which is integrated in NanoScope™ takes hotspot reports from tools such as OPC verification or design based metrology such as NGR2100^{TM}. It allows fast and interactive viewing of hotspot groups, alongside their design layout, and images from simulation and real wafers. Its functions of pattern and cell extraction help us to quickly identify repeating patterns among a large number of violations. Through regrouping, sorting, filtering, and re-classification, the Hotspot Pattern Analyzer guides effective review sampling and enables individual or group hotspot disposition and tracking.

The HPA is available in standard module and two advanced option modules.

2.1 Standard Module

1) Multi-format histogram views of hotspot groups, filtering, and statistics
2) Hotspot layout display – individual or group tile view, chip-map view
3) On-screen multiple layout pattern overlay, movement, and comparison
4) Individual or group hotspot disposition and status tracking
5) Wafer or mask image overlay with design layout

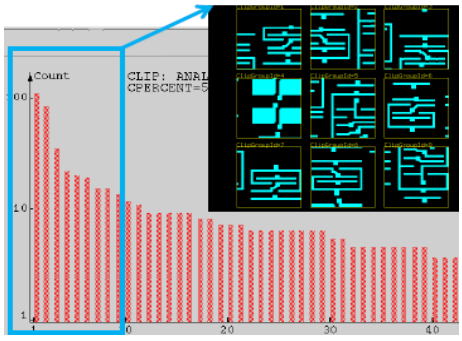

Figure 2. Multiple views of hotspot groups

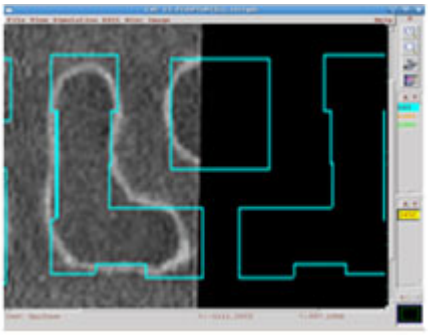

Figure 3. SEM image overlapped with design layout

2.2 Advanced Options

2.2.1 Pattern extraction module

Pattern extraction option module utilizes pattern matching and analysis techniques to re-group hotspots by localized layout or hierarchical design cells. It identifies and groups repeating patterns based on user selectable matching area.

1) Match and extract the same pattern groups on millions of locations in minutes
2) User definable extraction pattern area radius
3) Choices of orientation dependent pattern extraction and matching
4) Extract and rank patterns based on design hierarchy and cells
5) Greatly reduces large number of hotspots to smaller number of pattern and cell related groups
6) Identify and rank problematic repeating patterns and design cells

2.2.2 Pattern complexity extraction module

This option pre-groups a list of hotspots based on design pattern complexity and density around the vicinity of hotspot locations.

1) Separate and group hotspots between no design pattern areas and large pad areas
2) Separate and group hotspots based on the closeness to critical design patterns
3) Identify and rank hotspot severity based on local design pattern complexity
4) Identify criticality of hotspot based on locations of design patterns

2.3 Applications

- Design and pattern based hotspot review, individual or group hotspot disposition and status tracking
- Design and pattern based analysis of OPC verification results
- Design and pattern based analysis for results from layout process sensitivity checking
- Design and pattern based analysis, grouping, and filtering for hotspots detected in manufacturing
- Pattern based analysis of MRC results

3. DEFECT FILTERING

We have demonstrated defect filtering capability of HPA at the analysis of PWQ of metal layer in a NAND Flash memory and random contact hole patterns in a DRAM device.

3.1 Process Window Qualification of a metal layer

The full chip inspection capability of NGR2100^{TM} enables us to do PWQ of the whole features in a chip. Figure 4 shows the PWQ results of a memory device and the procedure for PWQ is as follows.

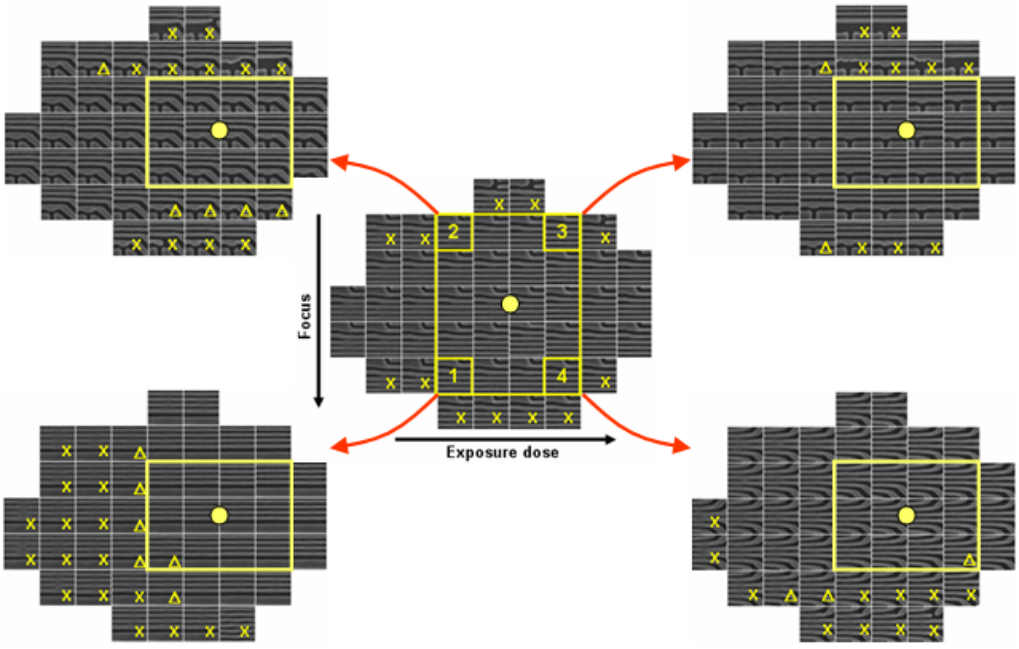

Figure 4. Process Window Qualification

1. Define a preliminary Process Window with some specific feature (Center of Figure 4).
2. Choose the 4 corner boundary fields of process window as Inspection fields to detect *Hot Spots (No 1~4 fields)*
3. Inspect the 4 corner boundary fields in RDI mode and review all the *Hot Spots* and select typical *Hot Spots* of each field.
4. Define Process Windows of each typical *Hot Spots* (4 corners of Figure 4)
5. Obtain *Real Process Window* by overlapping Process Windows of each *Hot Spots*

PWQ can help us to set the proper exposure condition and can give us the hot spot information to monitor for process control. Furthermore, the hot spot information would be sent to OPC or Design for correction to ensure wider process window.

In step 3, however, there might be so many Hot Spots found in those fields, because the 4 fields are all located at the edge of process window. So it would be very hard to select a few typical Hot Spots out of them. If we fail to identify the most critical Hot Spots, the process window obtained from this PWQ would appear somewhat wider than the real window and we may miss the chance to reinforce the critical Hot Spots.

Hot spot Pattern Analyzer has been evaluated to reduce the number of Hot Spots detected at step 4 by classifying into groups and to make it easier for us to select a few typical Hot Spots out of them. The histogram in Figure 5 shows the distribution of CD deviation of metal layer in NAND Flash memory from original design layout. X axis is CD deviation from the design layout and Y axis implies population of the measurement data. These data came from an under exposed field and bridging defects are most critical in this case. Since the points in the right side of the histogram are larger patterns than design layout, they are the most critical Hot Spots of bridging in this field. HPA analyzed these CD defects and selected 16 typical Hot Spots in the picture.

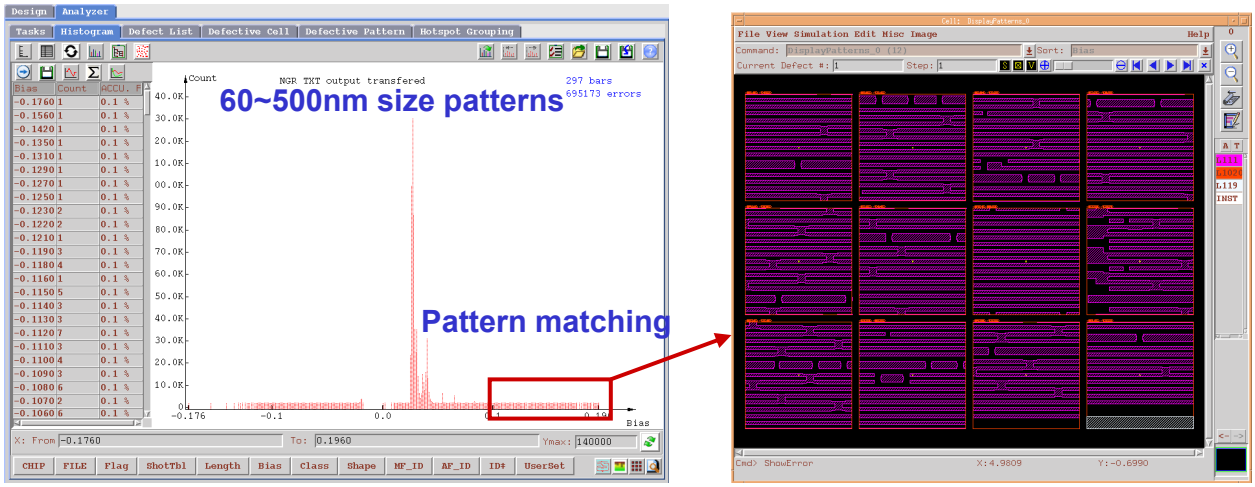

Figure 5. CD error distribution histogram and critical Hot Spots filtered at HPA

The information of these typical Hot Spots listed in the Figure 6 is sent back to NGR2100^{TM} for step 4 in PWQ. An example of process window of a critical Hot Spot is shown in the right side of Figure 6. These process widows of typical Hot Spots are overlapped to obtain the total process window of this process.

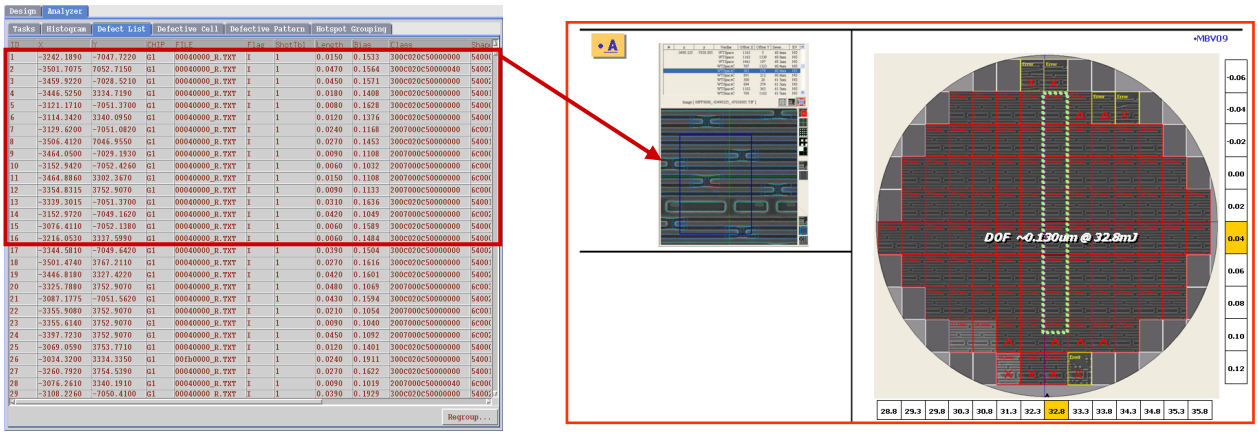

Figure 6. Typical Hot Spot lists and an example of process window of a critical Hot Spot

3.2 Random contact hole patterns in a DRAM device

HPA identifies and groups repeating patterns based on user selectable matching area. Its pattern matching principle is illustrated in Figure 7. If edge shift or resize of polygons are within tolerance, they are grouped together. It also extends into jog patterns within tolerance.

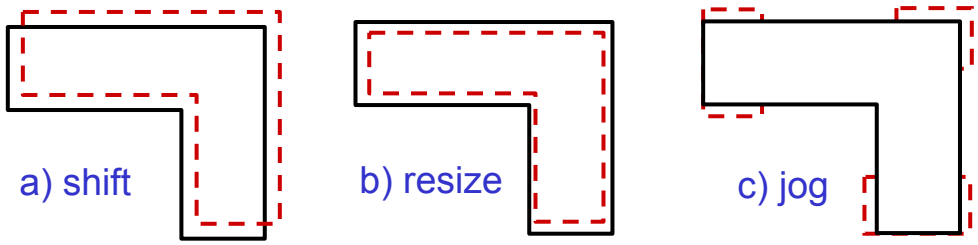

Figure 7. Edge and jog tolerance – a) edge shifted polygons, b) resized polygons and c) Polygons with jog length within tolerance are grouped together

Pattern grouping capability of HPA has been evaluated on random contact holes of a DRAM device. The disposition of random contact hole patterns is 2 dimensional and it is very difficult to classify them into groups. So it is very hard to feed back the measurement data of them to OPC for CD correction.

The histogram of CD deviation of random contact holes from original target is on the top of Figure 8. It is possible to select some region of interest for analysis. The left side of the histogram means smaller CD than target and typical layouts in this region are extracted from HPA. The typical layouts of other regions are extracted in b) and c) likewise. The result shows that dense array contact holes are on target, but semi-dense or linear array contact holes have large CD errors. In this case, the layout of random contact holes are corrected for targeting with model based OPC tool and the CD errors related with disposition of contact holes are analyzed by HPA for OPC feedback.

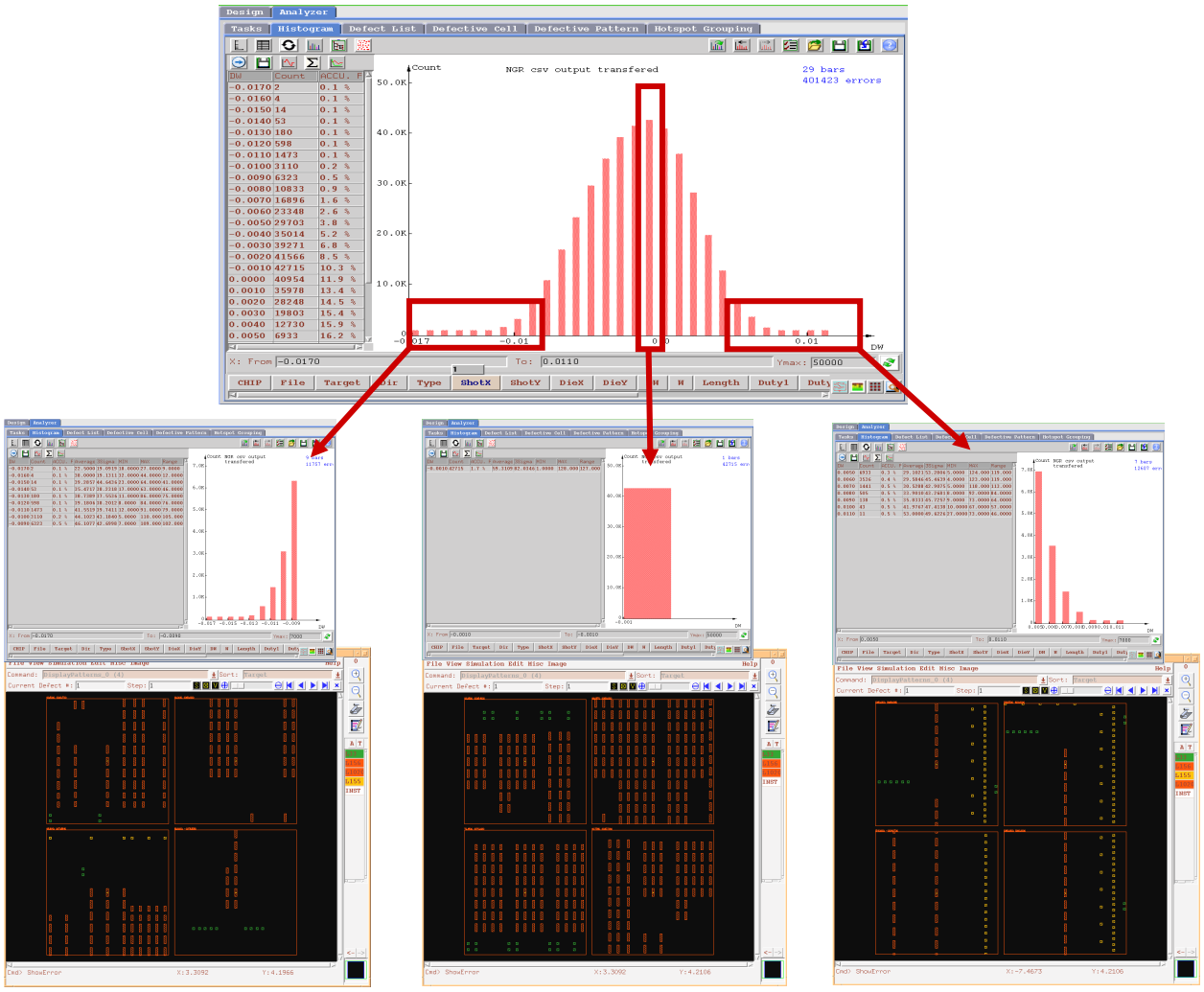

Figure 8. Histogram of random contact hole CD deviation. a) smaller CD than design layout, b) CD on target, c) larger CD than design layout

4. CONCLUSIONS AND DISCUSSIONS

- We have demonstrated systematic defect filtering and data analysis methodology for design based metrology.
- This method can classify measurement data from DBM into groups to reduce defect counts.
- Defect filtering capability has been evaluated at the analysis of PWQ of metal layer in a NAND Flash memory and random contact hole patterns in a DRAM device
- It was possible to group the Hot Spots of metal layer detected at PWQ and to select a few typical Hot Spots out of them
- Random contact hole layer of a DRAM device has been analyzed and CD errors related with disposition of contact holes were fed back to model based OPC

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