

Hot Spot Management through Design Based Metrology - Measurement and Filtering -

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ABSTRACT

Recently several Design Based Metrologies (DBMs) are introduced and being in use for wafer verification. The major applications of DBM are OPC accuracy improvement, DFM feed-back through Process Window Qualification (PWQ) and advanced process control. In general, however, the amount of output data from DBM is normally so large that it is very hard to handle the data for valuable feed-back. In case of PWQ, more than thousands of hot spots are detected on a single chip at the edge of process window. So, it takes much time and labor to review and analyze all the hot spots detected at PWQ. Design-related systematic defects, however, will be found repeatedly and if they can be classified into groups, it would be possible to save a lot of time for the analysis.

We have demonstrated an EDA tool which can handle the large amount of output data from DBM by classifying pattern defects into groups. It can classify millions of patterns into less than thousands of pattern groups. It has been evaluated on the analysis of PWQ of metal layer in NAND Flash memory device and random contact hole patterns in a DRAM device. Also, verification was tuned to specific needs of the designer as well as defect analysis engineers by use of EDA tool's 'Pattern Matching Function'. The verification result was well within the required specification of the designer as well as the analysis engineer. The procedures of Hot Spot Management through Design Based Metrology are presented in detail.

Key words: Design Based Metrology, pattern matching, pattern grouping, pattern classification

1. INTRODUCTION

1.1 Process control procedure

As the design rule of device approaches to its limit, the usable depth-of-focus and exposure latitude are becoming smaller and smaller. As IC industry developed 45nm node and beyond, OPC without considering process variation can't guarantee its accuracy. Typical photomask manufacturing process flow is made up by trial and error. Firstly, OPC step carried out. Of course, model for primary OPC should be prepared. Wafer process and inspection follow after OPC step, then inspection and analysis results are feed-back into OPC. This procedure is repeated until the results are satisfied. In this process, versatile and efficient analysis is the most important step to reduce unnecessary repetition and waste of time and cost. Wafer verification and analysis is divided into extracting wafer results(CD) and analysis of these results. The CD data should be accurate and abundant to obtain valuable analysis result. As pattern features are getting smaller, high resolution and throughput of measurement should be retained to obtain accurate CD value. So, noble OPC feedback methodology which can analyze a large amount of data by user-friendly way is required. Figure 1 shows the typical flow for manufacturing the photomask and the requirements.

In this paper, we will discuss the analysis process to improve efficiency of feedback.

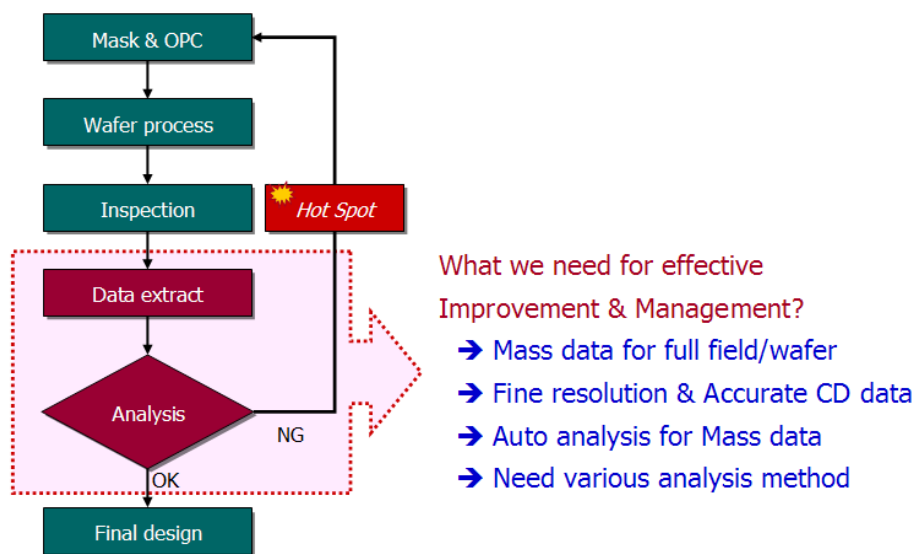


Figure 1. Process control flow

1.2 Design based Metrology tool - NGR2100™

A wide-field pattern inspection system which can compare the pattern on wafer to the design layout has been developed. NGR2100™ can compare the real printing images with designed target layout and measure the CD of all the features in a chip. It consists mainly of two parts, the hardware to acquire wafer images and the software to compare wafer images with CAD layout and analyze the edge placement error. The former is called Electron Image Acquiring System (EIAS) and the latter Geometry Verification Engine (GVE). The key feature of EIAS is the high-resolution and high-speed secondary electron acquisition capability to acquire images without field distortion over wide scan field. In short, NGR is a inline 2-Demantional CD-SEM using EIAS and GVE that inspect large area and measure large number of accurate CD data quickly. Overview of NGR2100 is displayed in Figure 2.

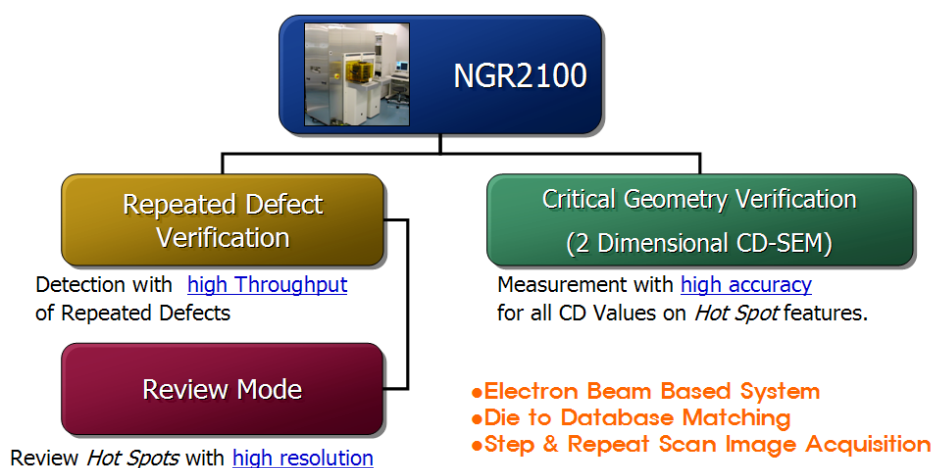


Figure 2. Overview of NGR2100™

GVE compares the target GDS layout with SEM images acquired at EIAS and detects systematic defects. The systematic defects are classified and grouped according to the geometry or shape of the features, and would be put on a DFM and APC platform. Due to the capability to cover the whole chip area with the high-resolution and high-speed, it would be the suitable verification tool for DFM and APC feed-back.

NGR2100™ has several verifiers to classify pattern features according to the shape and function in the DB. They are line end, corner, space width, line width, Gate on Active – measures Gate width on Active area – and so on. It is even possible to measure the overlay error between the two layers by comparing the centers of the image of each layer. This is illustrated on Figure 3 which shows the basic verifier of NGR 2100.

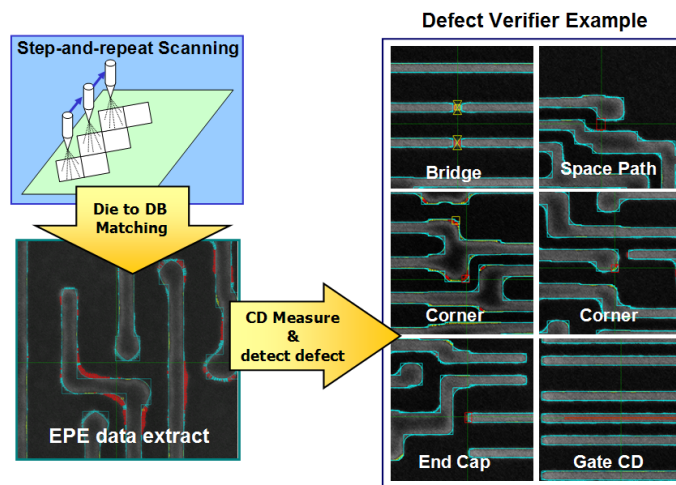


Figure 3. basic verifiers of NGR2100™

1.3 Analysis & Feedback - HPA

The Hotspot Pattern Analyzer (HPA) which is integrated in NanoScope™ takes hotspot reports from tools such as OPC verification or design based metrology such as NGR2100™. It allows fast and interactive viewing of hotspot groups, alongside their design layout, and images from simulation and real wafers. Its functions of pattern and cell extraction help us to quickly identify repeating patterns among a large number of violations. Through regrouping, sorting, filtering, and re-classification, the Hotspot Pattern Analyzer guides effective review sampling and enables individual or group hotspot disposition and tracking.

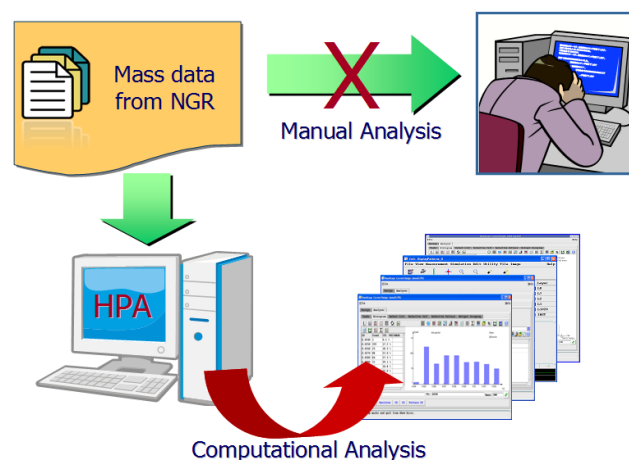


Figure 4. Overview of HPA

1.3.1 Applications

- Design and pattern based hotspot review, individual or group hotspot disposition and status tracking
- Design and pattern based analysis of OPC verification results
- Design and pattern based analysis for results from layout process sensitivity checking
- Design and pattern based analysis, grouping, and filtering for hotspots detected in manufacturing
- Pattern based analysis of MRC results

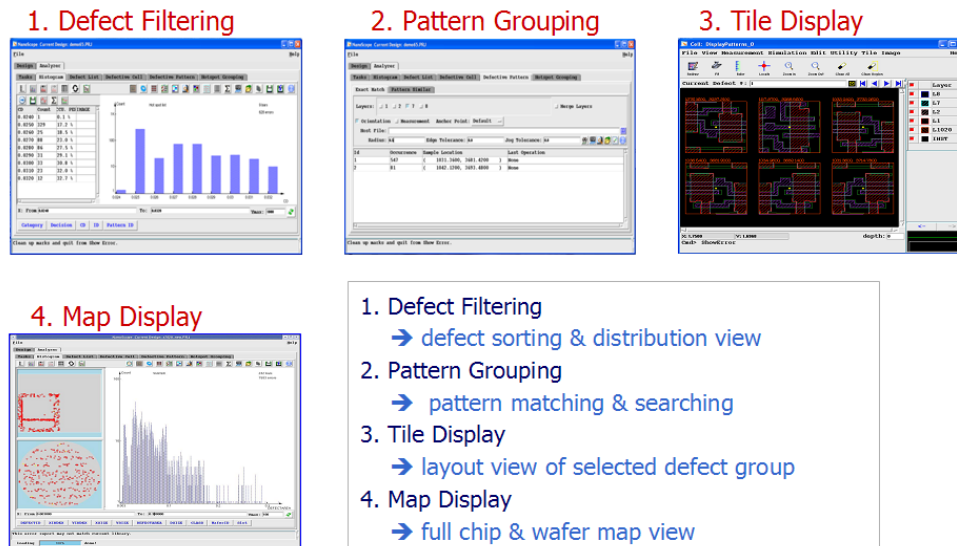


Figure 5. Basic functions of HPA

1.4 Schematic

As shown in the previous section, there are many advantages using a NGR for measurement tool and HPA for data analysis s/w. Figure 6 shows the flow chart to make analysis of mass data by combining their merit. As we use the powerful analysis functions of HPA to analyze mass data from NGR, the valuable information is provided to OPC engineer, Layout designer, Defect analyzer.

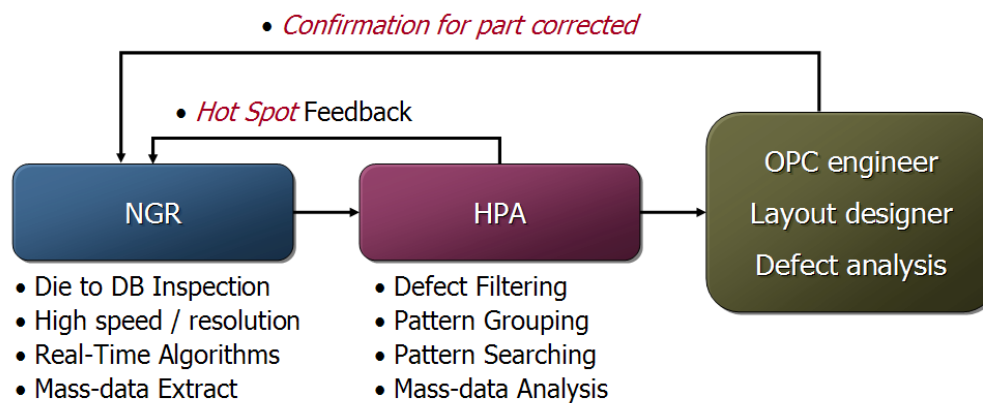


Figure 6. Combining NGR & HPA for effective analysis

2. EXPERIMENT

We have demonstrated application capability of HPA at the analysis of PWQ of metal layer in a NAND Flash memory and random contact hole patterns in a DRAM device.

2.1 Metal layer in a NAND Flash memory

2.1.1 Application to PWQ flow

The full chip inspection capability of NGR2100™ enables us to do PWQ of the whole features in a chip. PWQ can help us to set the proper exposure condition and can give us the hot spot information to monitor for process control. Furthermore, the hot spot information would be sent to OPC or Design for correction to ensure wider process window. However, there might be so many defects found in those fields, because inspection is running at marginal fields of EL or DOF during PWQ. So it would be very hard to select a few typical Hot Spots out of them. If we fail to identify the most critical Hot Spots, the process window obtained from this PWQ would appear somewhat wider than the real window and we may miss the chance to reinforce the critical Hot Spots.

Hot spot Pattern Analyzer has been evaluated to reduce the number of Hot Spots by classifying into groups and to make it easier for us to select a few typical Hot Spots out of them. The histogram in Figure 7-(b) shows the distribution of CD deviation of metal layer in NAND Flash memory from original design layout. X axis is CD deviation from the design layout and Y axis implies population of the measurement data. These data came from an under exposed field and bridging defects are most critical in this case. Since the points in the right side of the histogram are larger patterns than design layout, they are the most critical Hot Spots of bridging in this field. HPA analyzed these CD defects and selected 12 typical Hot Spots in the picture. The information of these typical Hot Spots listed in the Figure 7-(d) is sent back to NGR2100™ for full chip review. An example of process window of a critical Hot Spot is shown in Figure 7-(e). These process widows of typical Hot Spots are overlapped to obtain the total process window of this process.

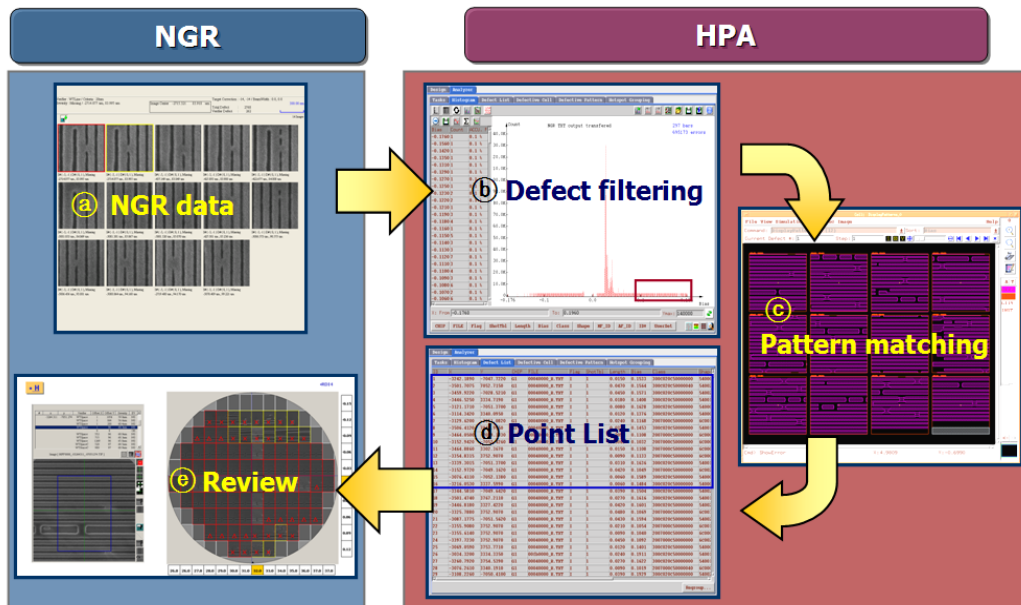


Figure 7. Application of HPA to PWQ process

2.1.2 Application to Multi die process

During PWQ process, there might be more than millions of defects found in each fields, because inspection is running at marginal field to check pattern which drop the DOF and EL margin. It is almost impossible to analyze the defects from many dies without computational system. In this situation, useful information can easily be obtained using HPA S/W. HPA can be helpful classify defects into systematic/random/unique group by analyzing disposition of pattern groups in each field. As shown in Figure 8-(d), group A is weak at (-)focus and group B is weak at (+)focus. Group C appears in the overall die and doesn't seem to be affected by focus.

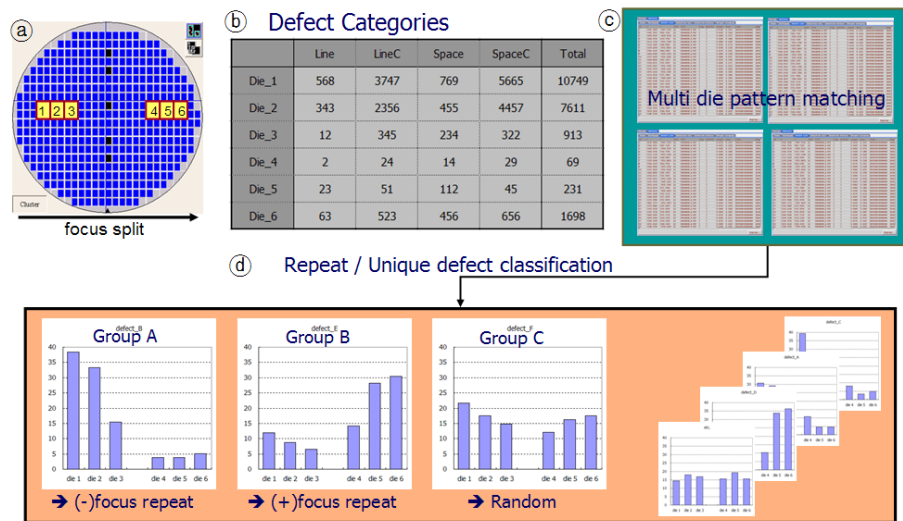


Figure 8. Multi die analysis using pattern grouping

2.2 Random contact hole

2.2.1 Problem with 2D pattern analysis

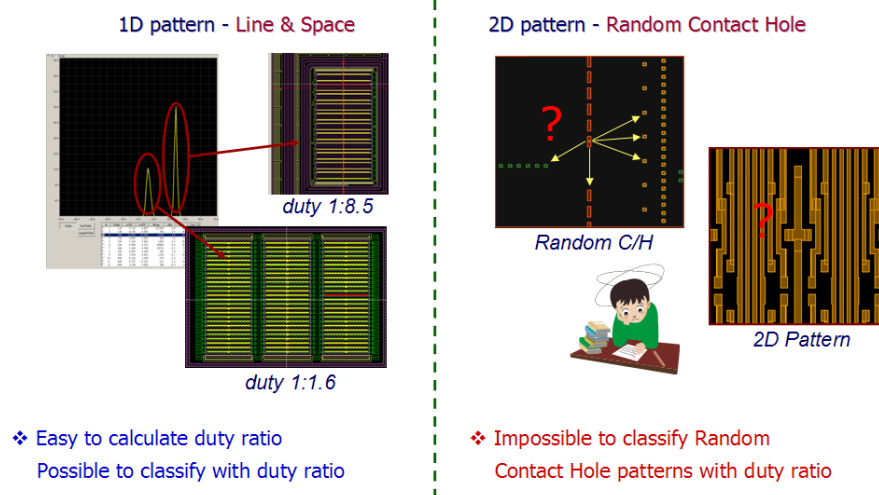


Figure 9. Problem with 2D pattern analysis

Because of the 2Dimensional disposition of random contact hole patterns, it is very difficult to classify them into groups. So it is also very hard to feed-back the analysis data to OPC engineer for CD correction. Since DRAM GATE consist of mainly Line & Space pattern, duty ratio is commonly used for classification of DRAM GATE. OPC feed-back can be carried out by classifying line & space pattern of DRAM GATE using duty ratio. In the left picture of Figure 9, inspected patterns are divided into two groups that have different duty ratio. In case where each group has different duty ratio, they could be corrected by OPC work. However, this approach has limited practical utility because 2D pattern doesn't have facing pattern edges in four directions. To eliminate this drawback, classification functions are required with various criterions for 2D pattern.

2.2.2 Analysis with Pattern Matching

The histogram of CD deviation of random contact holes from original target is on the top of Figure 10. It is possible to select some region of interest for analysis. The left side of the histogram means smaller CD than target and typical layouts in this region are extracted from HPA. The typical layouts of other regions are extracted in b) and c) likewise. The result shows that dense array contact holes are on target, but semi-dense or linear array contact holes have large CD errors. In this case, the layout of random contact holes are corrected for targeting with model based OPC tool and the CD errors related with disposition of contact holes are analyzed by HPA for OPC feed-back.

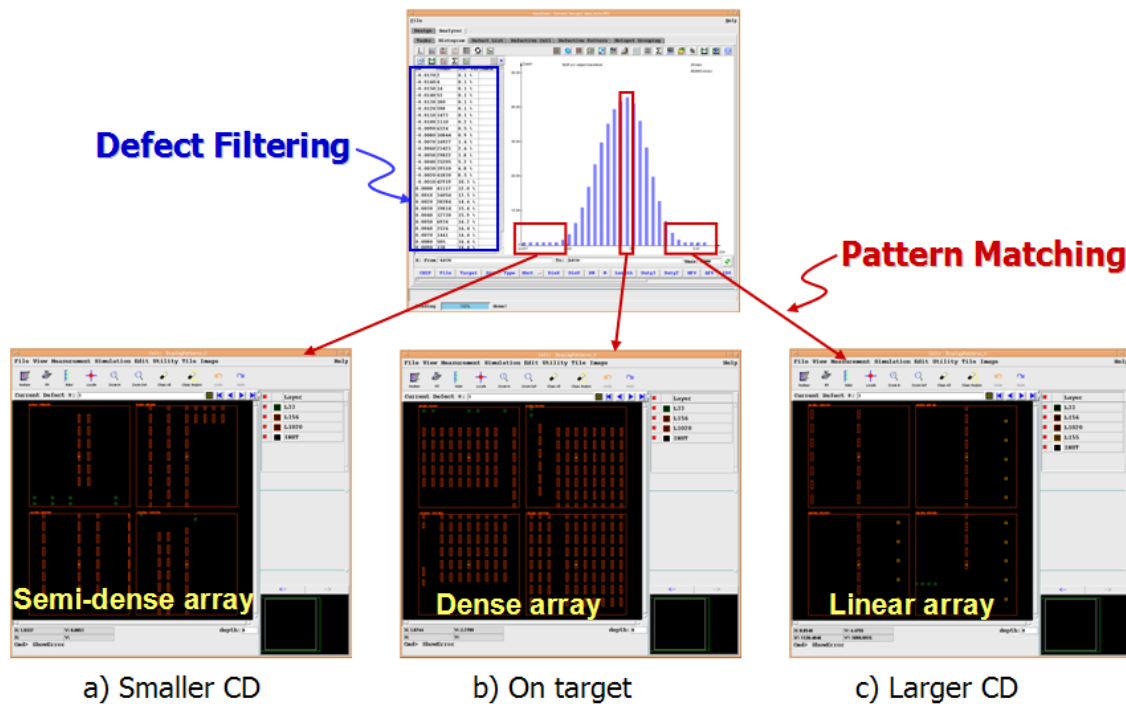


Figure 10. Analysis with Defect Filtering & Pattern Matching

2.2.3 Analysis with Location of Hot Spots

The location of the defect is also very valuable information. High erroneous region marked by rectangle from gathered data of Figure 11, shows regional proportion (C). This information showed that detected region had mask fabrication issue. So utilizing the location of the defect is useful in analyzing not only CD of the pattern but also quality of photomask, condition of scanner, process history.

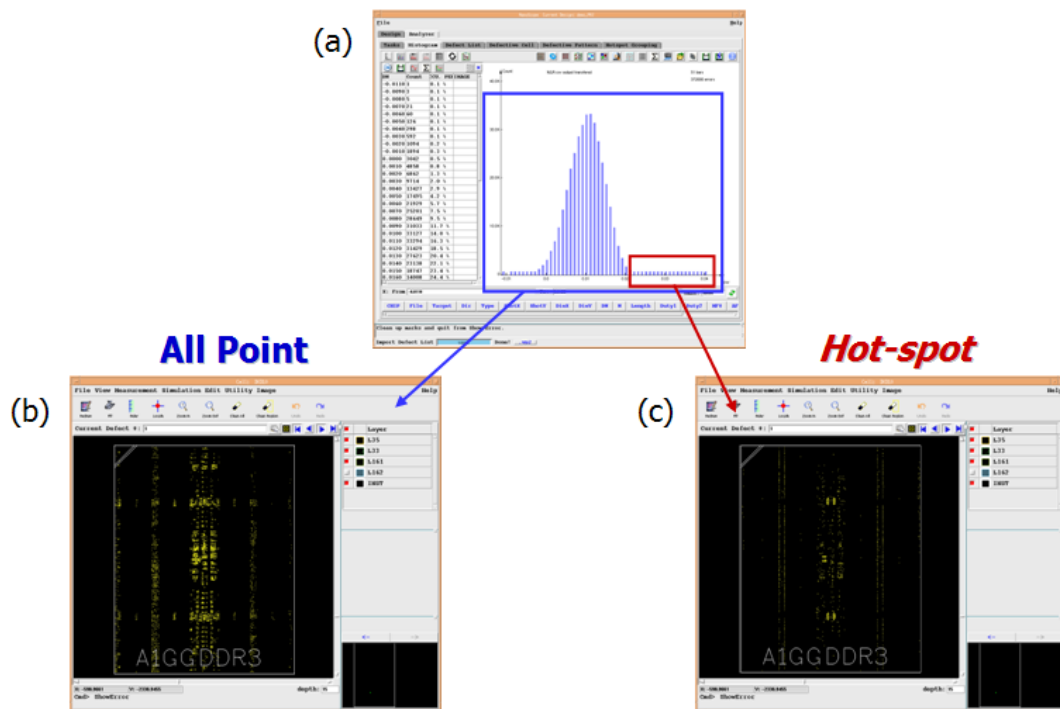


Figure 11. Hot-spot analysis using disposition of defects

2.2.4 Analysis with Distribution of Pattern Group

We should know about the distribution of each group throughout 'all error range' for CD tuning. The pattern group showing 2-peak, Figure 12-(a) should move and concentrate on target to improve CD uniformity. One important fact to consider when analyzing such data is not to look locally. Since the data can have uneven profile. In case where total distribution ignored, correction has limited practical utility because the defects in both peak move together. If don't consider overall distribution, all defects in field or chip move to small or large CD error. The method used in this section can help us to correct CD by visualizing the distribution of each group. The following explain the sequence to correct pattern that has distribution like Figure 12-(a) to (b) using pattern grouping function of HPA.

- 1) 1st pattern matching (coarse matching)
- 2) Analysis & correct each group
- 3) Select uncorrectable group
- 4) 2nd pattern matching (fine matching)
- 5) Analysis & correct

We demonstrate in Figure 12~14 more detail about analyze sequence using distribution show function of HPA.

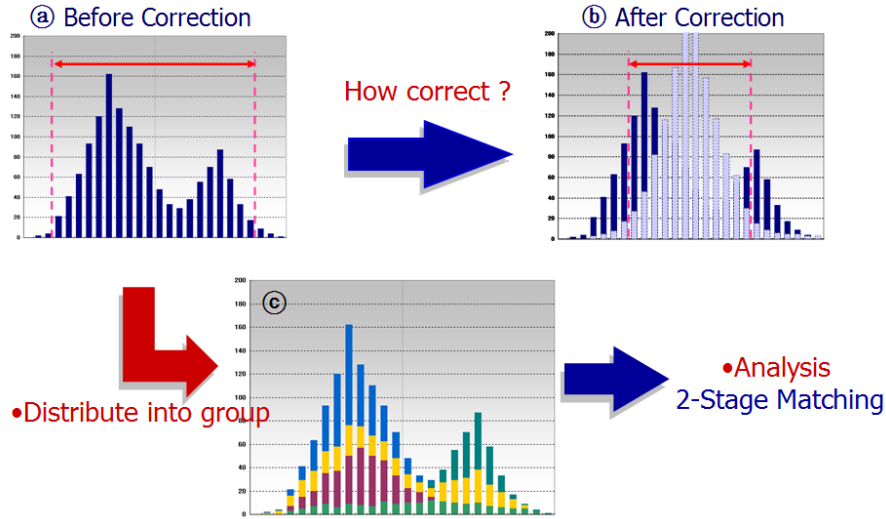


Figure 12. CD Verification flow of NGR2100™

First, divide target pattern into less than five groups using coarse matching. If there are many groups, we can do more accurate correction, but based on balance in accuracy and TAT, less than five groups are sufficient. In Figure 13, gathered data was first roughly divided into five groups according to their environment. Since group B, D, E are proportionally spread out they can easily be corrected, but Group A is widely distributed on x-axis and Group C has 2-peaks. Thus, correction can't be carried out by CD correction. We need further works for accurate analysis.



Figure 13. 1st Pattern Matching – Coarse Matching

Second pattern matching was done with Group C to complete the correction. As shown in left-top of Figure 14, Group C is a vertical linear hole pattern. If Group C is classified in more detail, they are divided into a semi-dense array and a linear array pattern group. The two newly identified groups could be moved to on-target position by correcting each group individually.

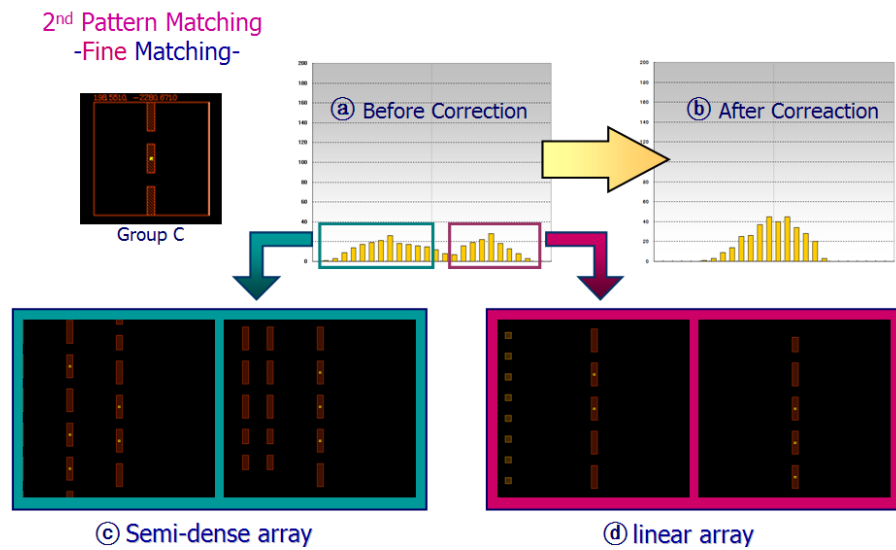


Figure 14. 2nd Pattern Matching – Fine Matching

2.2 Specific analysis

It is hard to find interesting pattern in the full chip DB because full chip data base is too large and complicated. One of the function of HPA, pattern search, is applicable to review of specific pattern in Design Library. Preformed Design Library has weak points in marginal field, process monitoring points, and critical patterns need special management by layout designer or PI engineer. Extracted point list from pattern search goes back to NGR for inspection or review, and the results can be used for pattern correction. Figure 15 shows the analysis flow of pattern search function.

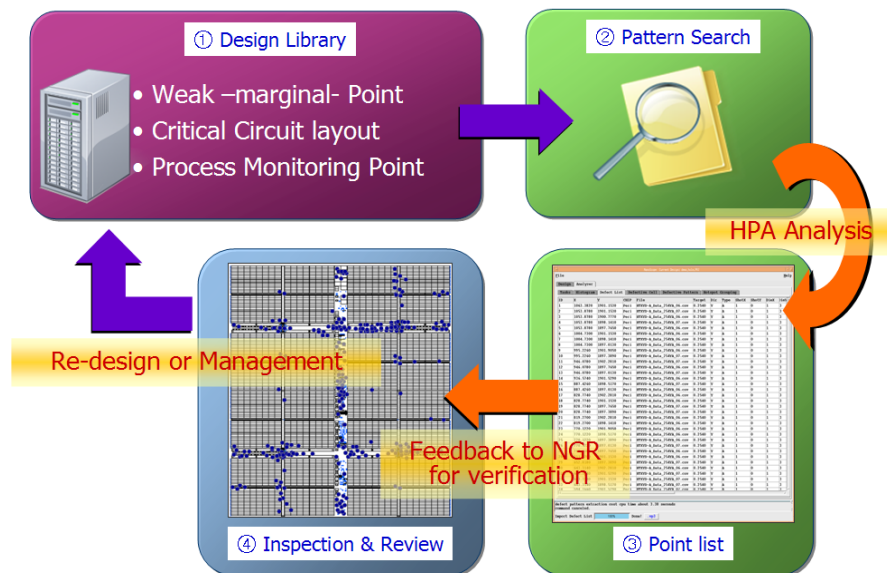


Figure 15. Specific pattern analysis using pattern search

3. CONCLUSIONS AND DISCUSSIONS

- We have demonstrated *hot-spot management* and *data analysis methodology* for DBM(design based metrology).
- This method can classify huge amount of measurement data from DBM into groups to reduce defect counts.
- *Hot-spot management* capability has been evaluated on the analysis of random contact hole layer in a DRAM device and multi chip PWQ data of metal layer in a NAND Flash.
- It was possible to filter the Hot Spots of metal layer detected at PWQ and random contact holes at DRAM GATE by grouping patterns with pattern matching technique.
- Pattern grouping of hole layer was done with two-stage matching method (Corse and Fine matching) to improve efficiency of analyzing data.
- Specific analysis of Design Library was carried out by pattern search function.

REFERENCES

1. Ryoichi Matsuoka et al., *New method for the quantitative evaluation of wafer pattern shape based on CAD data*, Proc. of SPIE vol. 5038, 2003.
2. Kunal N. Taravade et al., *Multichip reticle approach for OPC model verification*, Proc. of SPIE vol. 5256, 2003.
3. Hyunjo Yang et al., *OPC Accuracy and Process Window Verification Methodology for Sub-100nm Node*, Proc. of SPIE vol. 5375, 2004
4. Hyunjo Yang et al., *OPC Accuracy Enhancement through Systematic OPC Calibration and Verification Methodology for Sub-100nm Node*, Proc. of SPIE vol. 5752, 2005
5. Tadashi Kitamura et al., *Introduction of a Die-to-Database Verification Tool for the Entire Printed Geometry of a Die - Geometry Verification System NGR2100 for DFM*, Proc. of SPIE vol. 5756, 2005
6. Hyunjo Yang et al., *New OPC Verification Method using Die-to-Database Inspection*, Proc. of SPIE vol. 6152, 2006
7. Hyunjo Yang et al., *Advanced Process Control with Design Based Metrology*, Proc. of SPIE vol. 6518, 2007
8. Hyunjo Yang et al., *Wide Application of Design Based Metrology with Tool Integration*, Proc. of SPIE vol. 6922, 2008
9. Hyunjo Yang et al., *Systematic Defect Filtering and Data Analysis Methodology for Design Based Metrology*, Proc. of SPIE vol. 7272, 2009