OPC Verification and Hot Spot Management for Yield Enhancement through Layout Analysis

Gyun Yoo*[a], Jungchan Kim [a], Taehyeong Lee [a], Areum Jung [a], Hyunjo Yang [a], Donggyu Yim [a], Sungki Park [a], Kotaro Maruyama[b], Masahiro Yamamoto, [b] Abhisheck Vikram, [c] Sangho Park [d]

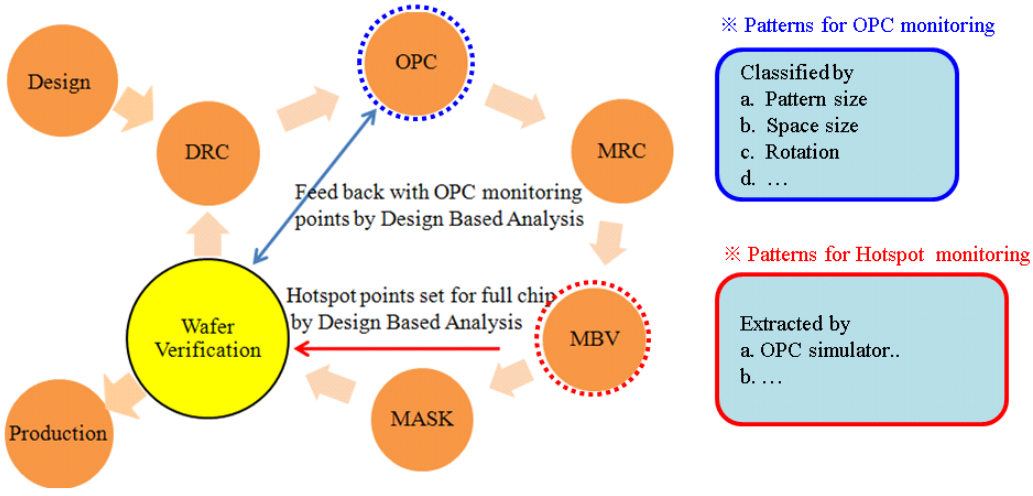
[a] Research & Development Division, Hynix Semiconductor Inc., Korea
[b] NanoGeometry Research, Inc., Japan [c] Anchor Semiconductor, Inc., USA
[d] DAOUXILICON, Inc., Korea

ABSTRACT

As the design rule shrinks down, various techniques such as RET, DFM have been continuously developed and applied to lithography field. And we have struggled not only to obtain sufficient process window with those techniques but also to feedback hot spots to OPC process for yield improvement in mass production. OPC verification procedure which iterates its processes from OPC to wafer verification until the CD targets are met and hot spots are cleared is becoming more important to ensure robust and accurate patterning and tight hot spot management.

Generally, wafer verification results which demonstrate how well OPC corrections are made need to be fed back to OPC engineer in effective and accurate way. First of all, however, it is not possible to cover all transistors in full-chip with some OPC monitoring points which have been used for wafer verification. Secondly, the hot spots which are extracted by OPC simulator are not always reliable enough to represent defective information for full-chip. Finally, it takes much TAT and labor to do this with CD SEM measurement. These difficulties on wafer verification would be improved by design based analysis. The optimal OPC monitoring points are created by classifying all transistors in full chip layout and Hotspot set is selected by pattern matching process using the NanoScope™, which is known as a fast design based analysis tool, with a very small amount of hotspots extracted by OPC simulator in full chip layout. Then, each set is used for wafer verification using design based inspection tool, NGR2150™. In this paper, new verification methodology based on design based analysis will be introduced as an alternative method for effective control of OPC accuracy and hot spot management.

Key words: Hot spot, OPC verification, Design based analysis



[Figure1] OPC verification flow

Metrology, Inspection, and Process Control for Microlithography XXV, edited by Christopher J. Raymond,
Proc. of SPIE Vol. 7971, 79710H · © 2011 SPIE · CCC code: 0277-786X/11/$18 · doi: 10.1117/12.870395

1. INTRODUCTION

1.1 OPC verification flow

1.1.1 Patterns for OPC monitoring

A pattern for OPC monitoring is used for wafer verification step to feed the OPC error back to OPC engineer. Optimal set of patterns for OPC monitoring can not only obtain high accuracy for TR targeting but, reduce the iteration of the cycle. However, a set of patterns for OPC monitoring which have been used for many years in wafer verification are not sufficient to feed-back information for various types of pattern in full chip into OPC engineer, and so there are some considerations to optimize its organization.

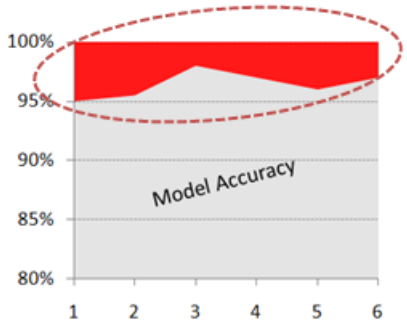
- Various types of pattern in full chip should be considered.
  (For example, Pattern size, Space to neighbor pattern and rotation of pattern is not enough criteria to classify entire patterns in full chip)
- Various types of Pattern in full chip should be optimally classified.
  (However, more criteria for classification causes time and labor loss in its process and wafer verification)
- Location of classified patterns in full chip should be considered.

1.1.2 Patterns for Hotspot monitoring

In the cycle, Model based verification carries out after OPC step. It has been proved as the powerful simulation system which can guarantee the quality of post OPC result and reduce the time loss with iterations of OPC verification flow. Even if an accurate model is necessary and the model is not always perfect, it provides an effective way to extract OPC error before mask manufacturing starts. However, as the design rule shrinks and pattern complexity increases, it seems that more data and effort are required for an accurate modeling and unpredictable hotspots are increasing. Since the model is not always perfect,

-.Hotspot which is extracted by OPC simulator has variation itself. (For example, 5% Error)
-.Patterns in similar environment with the hotspot (but, are not extracted by OPC simulator) have high possibility to be detected as a defect in wafer verification. (For example, because model has 95% Accuracy)

Therefore small amount of hotspots which are extracted by OPC simulator should be analyzed in full chip to cover the insufficient model accuracy and prevent the yield loss in the manufacturing.



[Figure 2] Insufficient model accuracy causes the increase of iteration and yield loss in manufacturing.

Since layout analysis provides us a capability of a fast processing and flexible modification with full chip layout, it is believed that layout analysis is a suitable approach for two ideas above. In this paper, improved OPC verification methodology based on layout analysis will be introduced as an alternative method for effective control of OPC accuracy and hotspot management.

2. LAYOUT ANALYSIS TOOL

The Hotspot Pattern Analyzer (HPA) which is integrated in NanoScope™ takes hotspot reports from tools such as OPC verification or design based metrology. It allows fast and interactive viewing of hotspot groups, alongside their design layout, and images from simulation and real wafers. Its functions of pattern and cell extraction help us to quickly identify repeating patterns among a large number of violations. Through pattern searching, sorting, filtering, and re-classification, the Hotspot Pattern Analyzer guides effective pattern classification and enables hotspot tracking.

2.1 Specific Functions

Specific functions of HPA used in this paper are as following.

User Define Pattern Search
Pattern Searching with GDS clip / Coordination
Pattern Grouping
Pattern Selection by distribution in Full chip

2.1.1 User Define Pattern Search

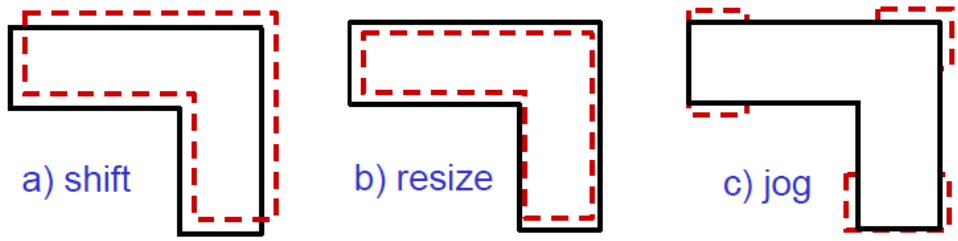
It provides the flexibility to do user defined rule-based pattern search. The length and direction of edges in the pattern are described by rules and HPA searches all the patterns in the design which matches with the condition specified by the user**.**

2.1.2 Pattern Searching with GDS clip / Coordination

The reference patterns are searched in the design library for exact match comparison then pixel based similar search carries out. It is also available to use the coordination with diameter as an input of pattern searching.

2.1.3 Pattern Grouping

Layout analysis tool identifies and groups repeating patterns based on user selectable matching area. Its pattern matching principle is illustrated in Figure 3. If edge shift or resize of polygons are within tolerance, they are grouped together. It also extends into jog patterns within tolerance. Pattern grouping capability of layout analysis tool enables us to classify huge amount of patterns to very small amount of them.



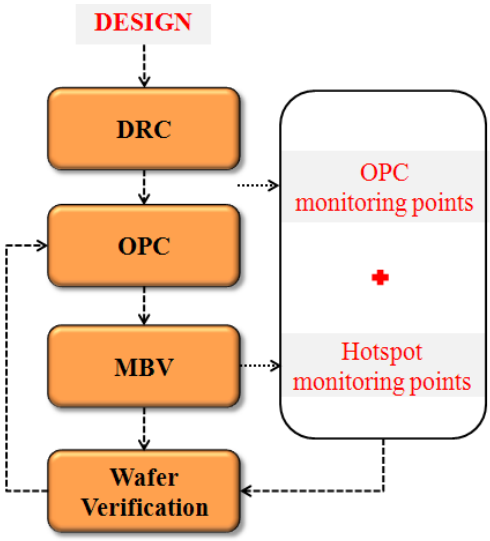
[Figure 3] Edge and jog tolerance – a) edge shifted polygons, b) resized polygons and c) polygons with jog length within tolerance are grouped together.

2.1.4 Pattern Selection by distribution in the full chip

Its function provides options for selection such as location in the full chip, random selection and total number of pattern and combination of pattern information to do sampling patterns. Dispersed patterns for one group which represents property of the full chip layout could be selected by those options.

3. CONCEPT OF LAYOUT ANALYSIS IN OPC VERIFICATION

Generally, OPC verification flow is similar with following figure 4. It starts from design rule cleared layout. OPC, model based verification and wafer verification follows next. The focus of improvement in new OPC verification flow is how well qualify the characteristic of full chip and feed-back into OPC on wafer verification step with OPC monitoring points and hotspot monitoring points.



[Figure 4] OPC verification flow

3.1 Pattern classification for effective OPC monitoring

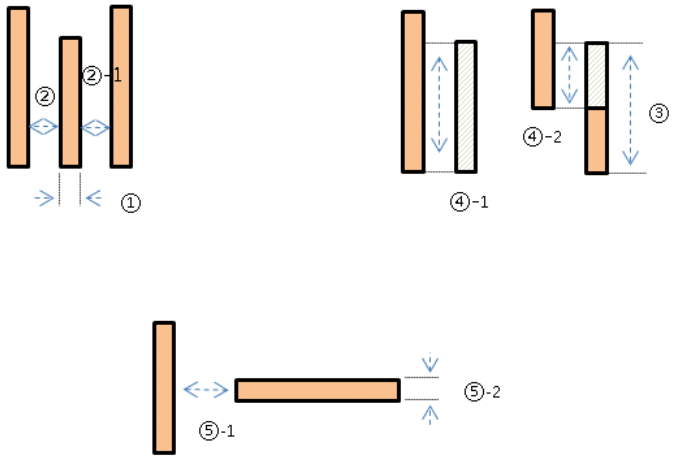
After design rule cleared, patterns which are met to "user define rule" are extracted to monitor the process characteristic of patterns in full chip. These are used in wafer verification step and to feed back to OPC engineer. It is called OPC monitoring points in this paper. A conventional pattern classification method has a simple rule such as pattern size and distance to neighbor pattern (Space). These are classified by rotation (Horizontal/Vertical). Therefore, four types of rule can be applied to classify patterns with conventional method. In order to guarantee characteristic of full-chip layout, the more rules, the better.

With new classification method, otherwise, environment which has different proximity effect on pattern needs to be concerned. It is not simple work but layout analysis tool enables us to make an idea applicable. Patterns which are extracted with new classification method refer to pattern grouping. It should be performed to effectively reduce the amount of duplicated candidates for OPC monitoring points. Some patterns vertically face to the neighbor pattern. These should be also considered with two conditions. One is distance between pattern and neighbor pattern and the other is size of the neighbor pattern. It is necessary to better describe the characteristic of patterns in the full chip layout because these types of environment have not been applied to classification so far even though these have some different optical proximity effect and process effect on the patterns.

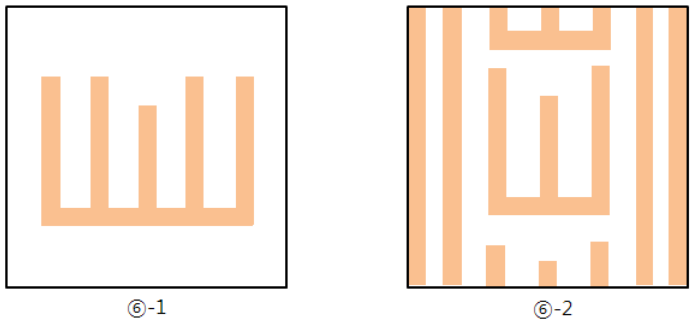
Ideas of pattern classification through layout analysis to extract OPC monitoring points are summarized in Table 1 and definition details of the rule which has been set up will be illustrated in Figure 5 and 6.

	Conventional	New Method through layout analysis
Rule	1. Pattern Size – (H/V) 2. Distance to the close Pattern (Space)	1. Pattern Size –(H/V) 2. Distance to the close Pattern 3. Pattern Length 4. Pattern Overlap Rate 5. Special Case (T- junction) 6. Pattern Density 7. Location of the OPC monitoring points in the full chip layout 8. …
Additional function	-	1. Pattern Grouping

[Table 1] Ideas of pattern classification through layout analysis to extract OPC monitoring points



[Figure 5] Details of "User Define Rule" 1) Pattern Size, 2) Distance to the neighbor pattern (Space), 3) Pattern Length, 4-1) Overlap rate [100%] 4-2) Overlap rate [50%], 5-1) Distance to neighbor pattern which vertically faces to the other, 5-2) Size of neighbor pattern which vertically faces to the other.

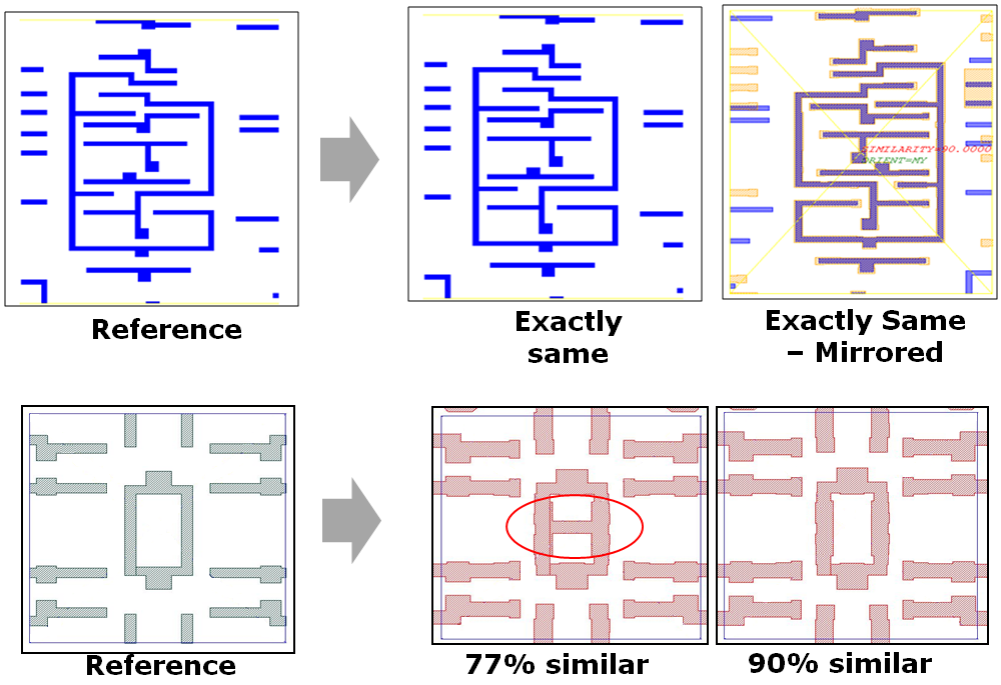


[Figure 6] Density is defined as 6-1) Density of pattern (less than 50%) 6-2) Density of Pattern (more than 50%)

3.2 Extension of a reference pattern for effective hotspot monitoring

MBV (Model Based Verification) is carried out before manufacturing mask. That is why post OPC layout should actually be hotspot cleared in MBV step. Since the model for MBV is accurate but not perfect, similar pattern with the reference hotspot need to be managed for wafer verification. Hotspots extracted by OPC simulator in this step are the reference of the Hotspot extension. It could cover variation of model accuracy in MBV step and effectively detect defects in wafer verification.

It is based on the 2 kinds of pattern matching method such as exact pattern matching and pixel based similar pattern matching. First of all, exactly same patterns with reference hotspot are extracted by pattern matching algorithm and pixel based similar matching algorithm. Figure 7 shows the example for two kinds of pattern matching algorithm.



[Figure 7] Pattern matching result 1) Exact pattern match 2) Pixel based similar pattern match

4. SET UP & RESULT

4.1 A set of patterns extraction for improved OPC monitoring

A set of patterns for OPC monitoring is extracted by pattern classification with both conventional method and new method through layout analysis on D4X GAT layer. Conventional rules such as pattern size, distance to neighbor pattern (Space) and rotation of pattern is applied to both method. New method through layout analysis includes newly defined rules such as pattern length, overlap rate, pattern density and special case (T-junction). Details of test conditions are as following table 2.

	Conventional Method	New method through layout analysis
1.Pattern Size	0~300nm	
2.Distance to Neighbor Pattern	1:5 (Pattern size : Distance to neighbor pattern)	
3.Rotation	Horizontal/Vertical	
4.Pattern Length		0nm~2000nm
5.Overlap Rate		≥ 50%
6.Pattern Density		0~100%
# Special Case 7.Distance to neighbor pattern which is vertically overlapped		0~500nm
8.Neighbor Pattern Size which is vertically overlapped to pattern		0~500nm

[Table 2] Experiment Condition for OPC monitoring point extraction

4.1.1 Result of patterns extraction for improved OPC monitoring

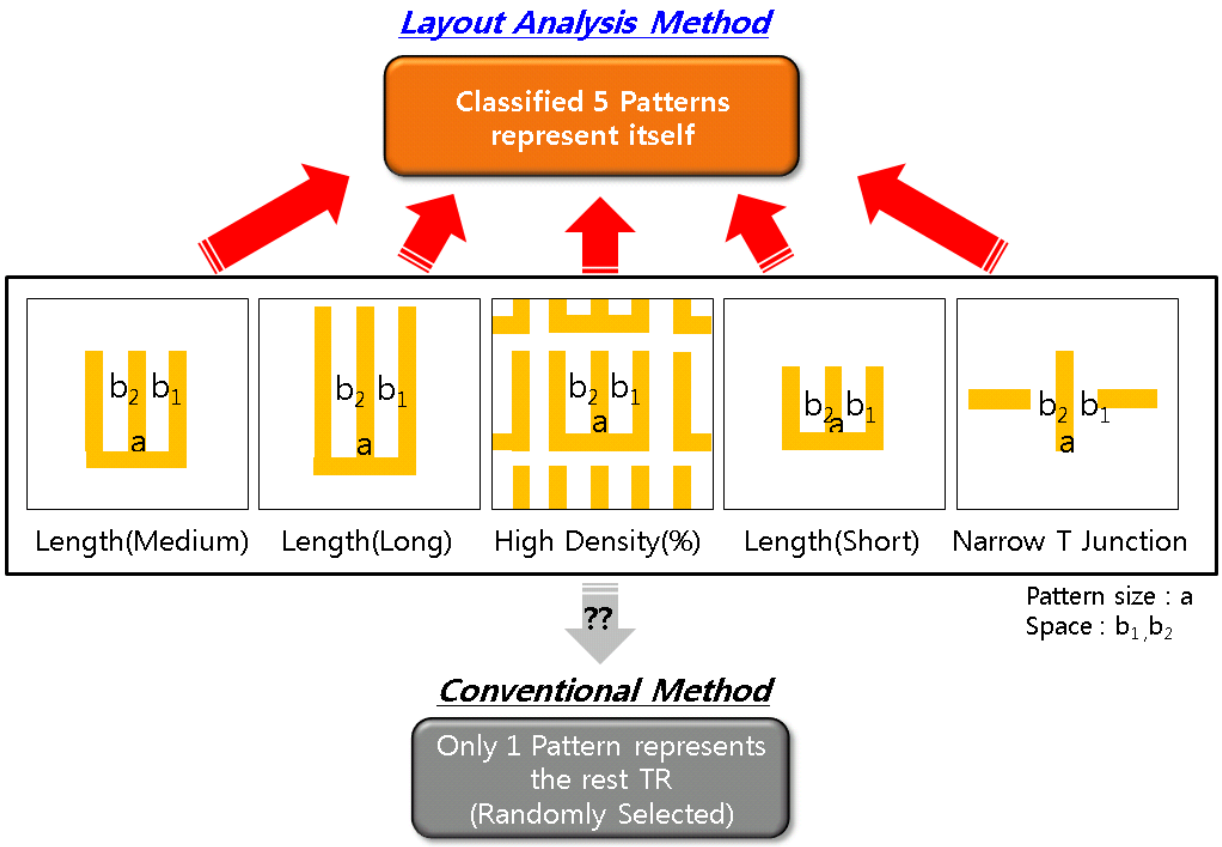
Time consumption to extract OPC monitoring points is reduced approximately 7.5times by layout analysis. Of course, total number of patterns in full chip layout is same for both conventional method and new method through layout analysis. However, number of selected patterns among candidates for OPC monitoring points is different. Selected patterns by new method are approximately extracted five times more than the other with conventional method. Table 3 shows the summary of the result.

	Conventional	New method through layout analysis
Running Time	**~15hrs**	**≤ 2hrs**
No. of total Patterns	**A×1M(ea.)**	**A×1M(ea.)**
No. of Selected Patterns for each category	**A(ea.)**	**5×A(ea.)**

[Table 3] Result for a set of patterns extraction for OPC monitoring with conventional method & new method through layout analysis

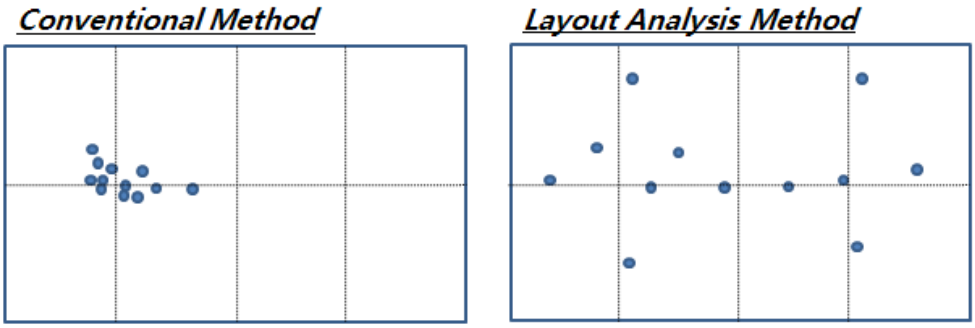
Increasing number of selected patterns for OPC monitoring results increasing TAT in wafer verification step but it can be offset by TAT reduction in Running Time for pattern classification. It enables us to feedback information of patterns in full chip layout for effective control of OPC accuracy without TAT loss.

Otherwise, the result also show us that one pattern has approximately represented five types of pattern even though it has a different process effects on each type of patterns such as optical proximity effect. The result is illustrated in figure 8.



[Figure 8] A description for a different number of selected patterns:
Pattern size (a), Space size (b) and rotation(vertical) of pattern is same for 5 types of pattern

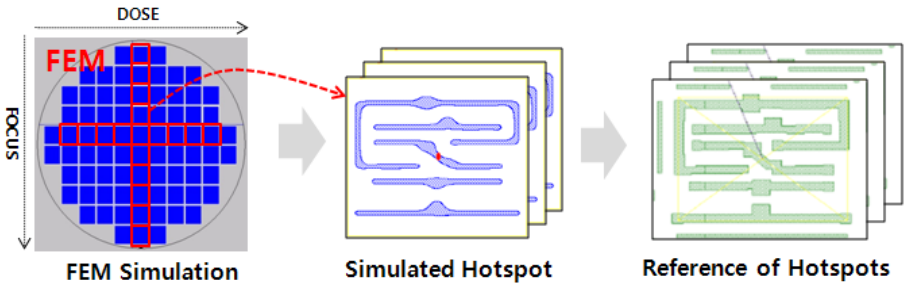
A distribution of selected pattern in full chip layout with both conventional and new method through layout analysis is shown in figure 9. The result shows that wafer verification with OPC monitoring points extracted with new method could reduce the possible feed-back error in a restricted area and cover the process variations in the full chip.



[Figure 9] 9-1)Location of OPC monitoring points with conventional method 9-2) Location of OPC monitoring points with new method in the full chip layout

4.2 A set of patterns extraction for efficient Hotspot monitoring

Hotspot extension is carried out on D4X GAT layer. The reference of hotspots is extracted by OPC simulator under FEM condition. Pattern searching is started with 3 references of hotspot. An experiment is preceded with two pattern searching methods of layout analysis tool and the result is classified by rotation and similarity. Details of test condition are as following figure 10.

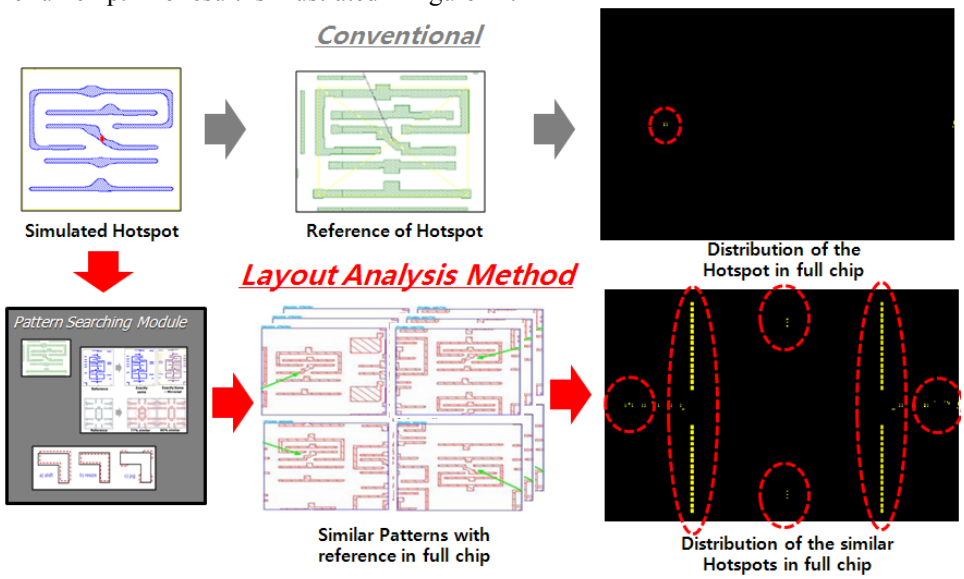


	Hotspot extraction through layout analysis
1.No. of reference Hotspot	3(ea.)
2.Pattern Search Method	Exact match, Similar match
3.Rotation	Mirrored X,Y , 0~360°
4.Size of hotspot (for layout)	1.0um (Diameter)
5.Similarity	≥ 90%

[Figure 10] Details of test condition for hotspot extension

4.2.1 Result of patterns extraction for efficient Hotspot monitoring

It takes very short time to search similar patterns with reference hotspot in full chip. It is less than a minute per one hotspot. Total number of hotspots is around 1K (ea.) in this test. The result shows that wafer verification with extended hotspots after selection by location could reduce feed-back error in a restricted area and cover the model variations in the full chip. The result is illustrated in figure 11.



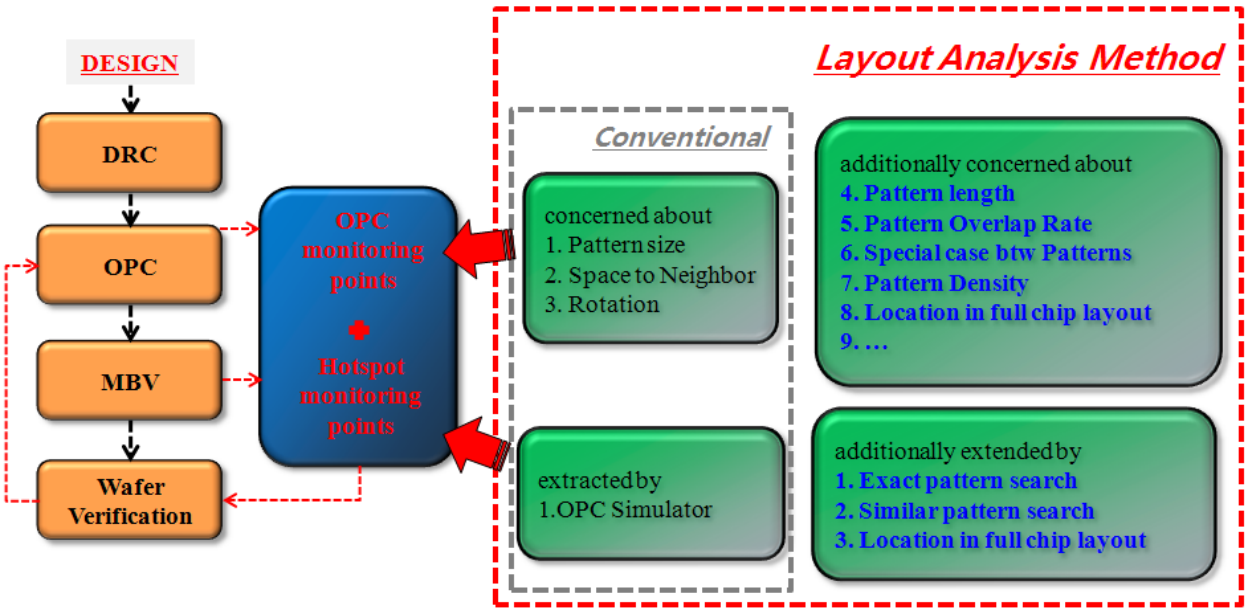
[Figure11] Distribution Map for hotspots extracted by pattern search through layout analysis

	Hotspot extraction through layout analysis
Running Time (min /1hotspot for full chip)	**≤ 1min**
No. of Hotspots (Exact + Similarity ≥ **90%**)	**~1000(ea.)**

[Table 6] Results for hotspot extension test

5. CONCLUSION

The possible improvement of OPC verification flow with layout analysis has been demonstrated successfully. However, User define rule for pattern classification needs to keep developing for higher feed-back accuracy because there might be some cases which are not able to cover with the new method or might be some ideas such as interaction to the other layers. Finally, the improved OPC verification flow is summarized in following figure 12.



[Figure 12] Improved OPC verification flow through layout analysis

- Improvement for OPC monitoring points and hotspot monitoring points has been demonstrated.
- Pattern classification for OPC monitoring points is complicate but applicable by layout analysis.
- Its result shows that various types of pattern have been grouped together so far and these should be managed with unduplicated categories.
- The new method for pattern classification includes various types of rules such as pattern size, space to neighbor, rotation of pattern, pattern length, overlap rate between two patterns, special case between two patterns, pattern density and its location in full chip layout. It needs to keep developing.
- It was possible to search similar patterns with reference of hotspot, distribute and select hotspots from the result of pattern searching.
- Hotspot points for wafer verification need to be extended because it could reduce feedback error caused by model variation and its location in full chip layout.
- It allows that better efficiency and accuracy to feed OPC error and hotspot information back without TAT loss.

REFERENCES

1. Ryoichi Matsuoka et al., *New method for the quantitative evaluation of wafer pattern shape based on CAD data*, Proc. of SPIE vol. 5038, 2003.
2. Kunal N. Taravade et al., *Multichip reticle approach for OPC model verification*, Proc. of SPIE vol. 5256, 2003.
3. Hyunjo Yang et al., *OPC Accuracy and Process Window Verification Methodology for Sub-100nm Node*, Proc. of SPIE vol. 5375, 2004
4. Hyunjo Yang et al., *OPC Accuracy Enhancement through Systematic OPC Calibration and Verification Methodology for Sub-100nm Node*, Proc. of SPIE vol. 5752, 2005
5. Tadashi Kitamura et al*., Introduction of a Die-to-Database Verification Tool for the Entire Printed Geometry of a Die - Geometry Verification System NGR2100 for DFM*, Proc. of SPIE vol. 5756, 2005
6. Hyunjo Yang et al., *Advanced Process Control with Design Based Metrology,* Proc. of SPIE vol. 6518, 2007
7. Hyunjo Yang et al., *Wide Application of Design Based Metrology with Tool Integration,* Proc. of SPIE vol.6922, 2008
8. Hyunjo Yang et al., *Systematic Defect Filtering and Data Analysis Methodology for Design Based Metrology,* Proc. of SPIE vol. 7272, 2009
9. Taehyeong Lee et al., *Hot Spot Management through Design Based Metrology-Measurement and Filtering* -, Proc. of SPIE vol.7520, 2009
10. Hyunjo Yang et al., *Systematic and Random Defect Control with Design Based Metrology,* Proc. of SPIE Vol. 7638,2010