

Smart Review Sampling Methodology in Huge Inspection Results

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The performance of defect inspection results for advanced technology nodes have extreme high defect counts frequently. The defect Pareto get high false rate due to the SEM non-visual defects, nuisance defects, or dummy fill patterns by traditional review sampling methodology. An integrated smart review sampling methodology is proposed to resolve the high false rate issue and dig out the DOIs and POIs effectively in huge big inspection results with aid of design data base.

Introduction

As technology node shrinks to 50nm and beyond, the performance of defect inspection may often result in above 10k defect counts on a single wafer, these defect data combine with systematic, random defects or high nuisance issue. It is hard to identify the defect Pareto by traditional defect randomly sampling methodology; i.e. 50 to 100 defects are reviewed on review SEM (scanning electron microscope). As a result, it will miss the important systematic or killing defects and further lead to an inevitable costly expense in the preliminary pi-run stage of device product. Several defects sampling methodologies (1-4) are proposed to screen out the non-killing defects. Sang Chong *et al.* (1) used the iDO function in KLA inspection tool which allows the user to arrange the detected defects into bins and then review the classified bins to reduce the nuisance. Scott Jasen *et al.* (2) adopted the design base binning (DBB) couples layout information from design data with the relative location of each detected defect, they can group the defects located at similar patterns by Design Based Grouping (DBG), or filter out the non-critical patterns by Design Based Classification (DBC), and use the mathematical model to calculate the defects size and locations at risk area by Defect Criticality Index (DCI). Yoshiyuki Sato *et al.* (3) also demonstrated that more yield-relevant defect Paretos can be created after SEM review by using DCI methodology. J. H. Yeh *et al.* (4) proposed to use pattern search engine to correlate defect of interests (DOI) to its pattern background. Various SEM review sampling methodologies mentioned as above are implemented to filter out the non-killing defect and find out yield impact DOIs.

The aim of this paper is to propose an integrated solution for smart SEM review sampling methodologies with aid of design database to resolve traditional defect randomly sampling issue in huge inspection results; we combined the location/size/gray level/area/design rule/pattern density/risk factor information of defects and defect locations with design base layout information to find out the yield-relevant killing or systematic defects.

Experimental:

Various smart review sampling methodologies are implemented on different products by different cases; After the KLA2830, Puma9550, or e beam inspections, the defects information are loaded into Nanoscope HPATM (Hotspot Pattern Analyzer) to do the smart sampling procedure with aid of layout database, then use e-beam review tool to review by specified location, size, risk area, POIs (pattern of interests). As compared to traditional defect randomly sampling methodology; i.e. 50 to 100 defects are reviewed directly on review SEM after inspection, smart review sampling methodologies includes defect criticality index, pattern density, pattern uniformity, risk factor, design rule, and size classification are implemented to resolve different conditions and cases for finding killing defects and systematic hot spots. Figure 1 illustrates the various smart review sampling methodologies as compared to traditional random review sampling methodology.

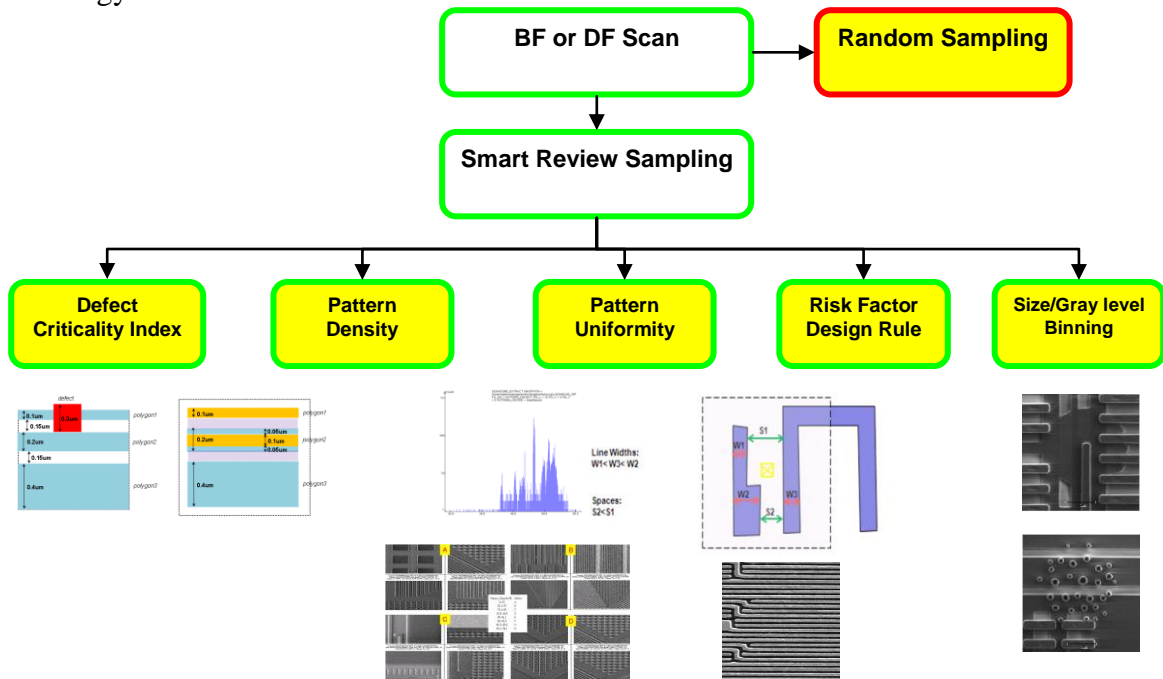


Figure 1 Illustrates the different smart review sampling methodologies.

Results and Discussion

Characteristics of Defects Information Correlate with Risk Patterns

A known suspected killing defect type at the specified sites will induce Icc standby electrical issue, therefore, we use the HPATM pattern search engine to search the POI location sites in a chip. Figure 2(a) indicates the killing peeling defect, and the figure 2(b) demonstrates the search results of POIs. Furthermore, the second step is to do the superposition correlation between the KLA scan defects results and POI in each die, as shown in figure 3. Figure 4(a) indicates that the KLA inspection defect counts are around 50000ea, and the review results found two defects of interest (DOIs) after 55ea traditional random review sampling. In contrary to traditional review methodology, figure 4(b) shows only 2973 ea defects are correlated to the specific POIs after screening the non-

correlated sites, and the review results found 17 ea DOI after 55ea review action within these correlated defects. Figure 5(a)(b) demonstrate the wafer map of Icc standby failure item after wafer final testing, the edge of wafer sort map shows far away from the general performance of Icc standby current ($40\mu\text{A} \sim 50\mu\text{A}$), and highly matches with the signature of smart sampling results, as shown in Figure 4(b).

Smart Review Sampling by Pattern Density on FEM Printed Wafer

Usually, we use the hot scan mode in the FEM printed wafer for getting high sensitive results, million of defects need to be identified and classified after scan. Therefore, smarter sampling becomes more important in such application. Smart review sampling by pattern density analysis is implemented to find out the systematic DOIs. Pattern density calculation is defined as following formula 1.

$$\text{Pattern Density Index} = (\text{Patterned Area}) \text{ in assigned Area} / \text{Total Assigned Area} \quad (1)$$

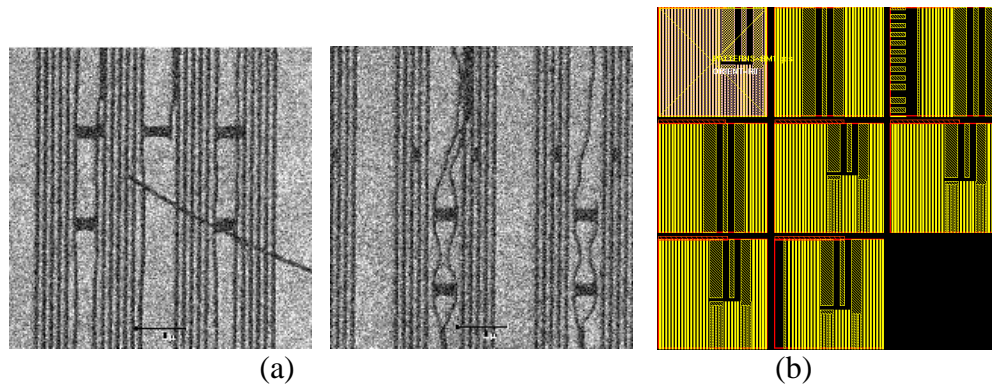


Figure 2 (a) Peeling defects induce Icc standby failure. (b) Patterns of interest (POI) in the pattern search process.

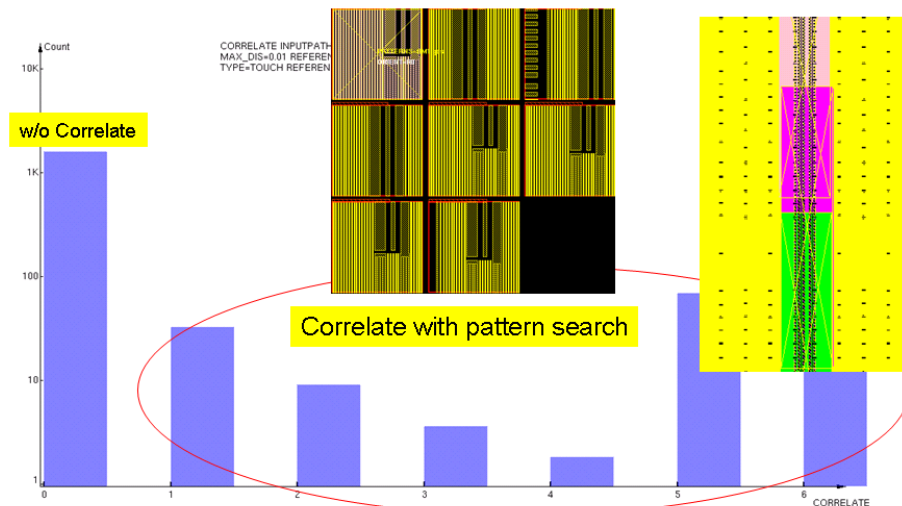
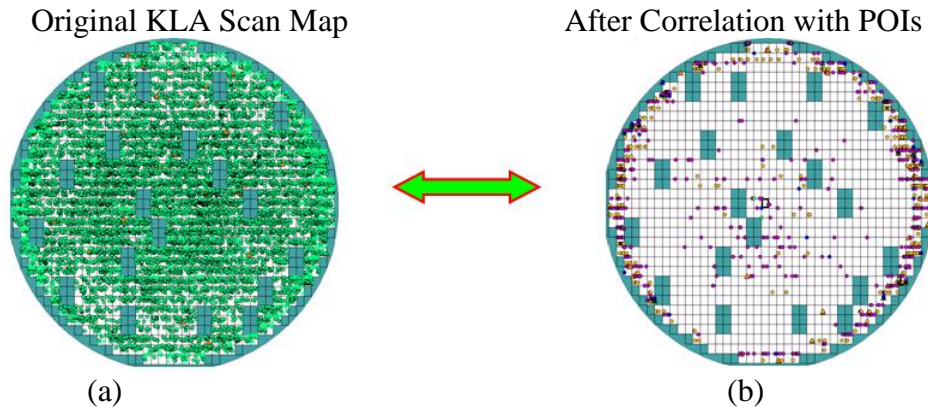


Figure 3 KLA Scan results superpose with POIs and find out the correlation.



Figures 4(a) Original KLA defect map (>5000ea defect counts) (b) After smart sampling filtering (2973 ea defect counts).

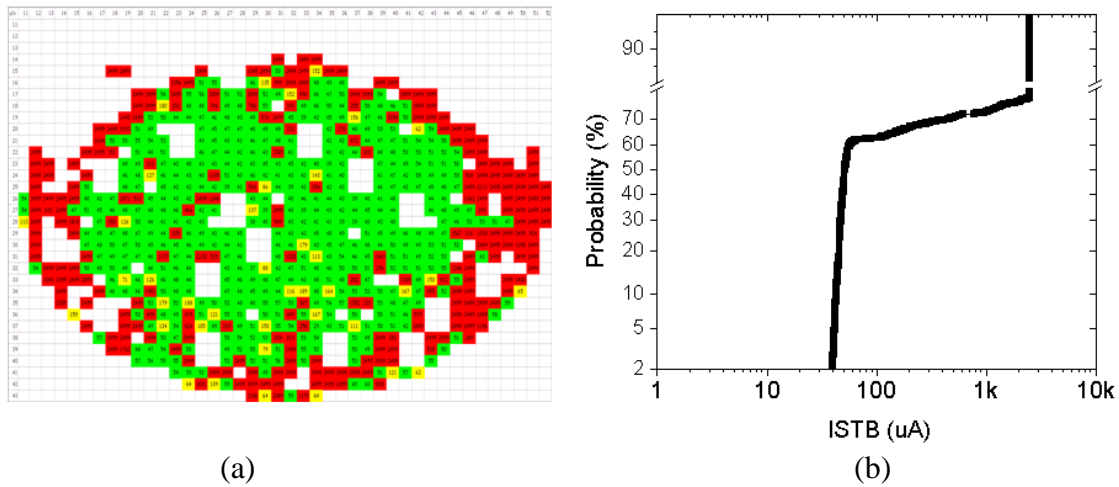


Figure 5 (a) demonstrates the wafer sort map of final testing, the red marks indicate the Icc standby failure bin. (b) Probability plot of Icc standby test in the same wafer.

Figure 6 illustrates the pattern density index versus defect classification review results, it indicates that pattern density locates 59~ 63% have higher risk for systematic defect in FEM printed wafer. The higher density area means the open area is larger than other area. Therefore, it is hard to find killing defects.

Beside these methodologies, we can use the defect criticality index, risk analysis factor according design rule, pattern uniformity, or the characteristics of defect information, etc.; then matches with design base to do the smart SEM review sampling to find out the DOIs and POIs. Furthermore, we can combine several smart sampling methodologies simultaneously from HPATM tool to find out the DOIs and POIs, as shown in Figure 7.

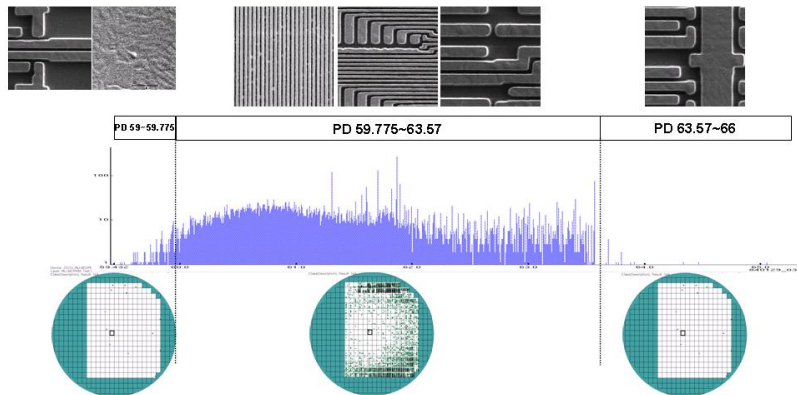


Figure 6 illustrates the pattern density index versus defect classification review results.

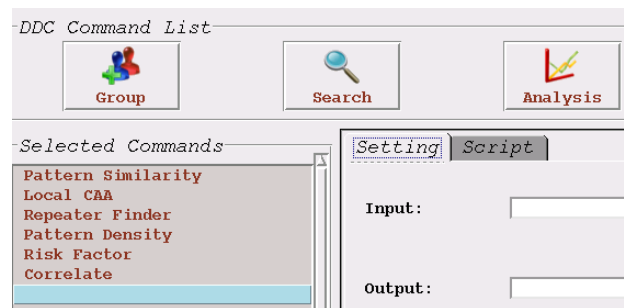


Figure 7 combine several sampling methodologies simultaneously to find out the DOIs and POIs.

Conclusion

Here demonstrates an integrated solution for classifying and digging out the killing or systematic DOIs and POIs effectively in huge big inspection results with aid of design data base. We can design the review sampling methodologies according the situation of inspection results, or integrate with several filtering methods to screen out the non-correlated defects and find out the yield-relevant killing or systematic hot spots. Therefore, the quality of the defect Pareto can be improved significantly.

References

1. Sang Chong, Eric Rying, Alexa Perry, Stephen Lam, Mary Ann St Lawrence, Andrew Stamper, *Advanced Semiconductor Manufacturing Conference (ASMC)*, p. 67 (2007).
2. Scott Jansen, Glenn Florence, Alexa Perry, Steven Fox, *Advanced Semiconductor Manufacturing Conference (ASMC)*, p. 69 (2008).
3. Yoshiyuki Sato, Yasuyuki Yamada, Yasuhiro Kaga, Yuuichiro Yamazaki, Masami Aoki, David Tsui, Chris Young, Ellis Chang, *Proc. of SPIE*, **6922**, 692213 (2008).
4. J. H. Yeh, and Allen Park, *Proc. of SPIE*, **6521**, 652114 (2007).